

Compal Confidential

EA50_HWS M/B Schematics Document

Intel Shark Bay SV (Haswell+ Lynx point)

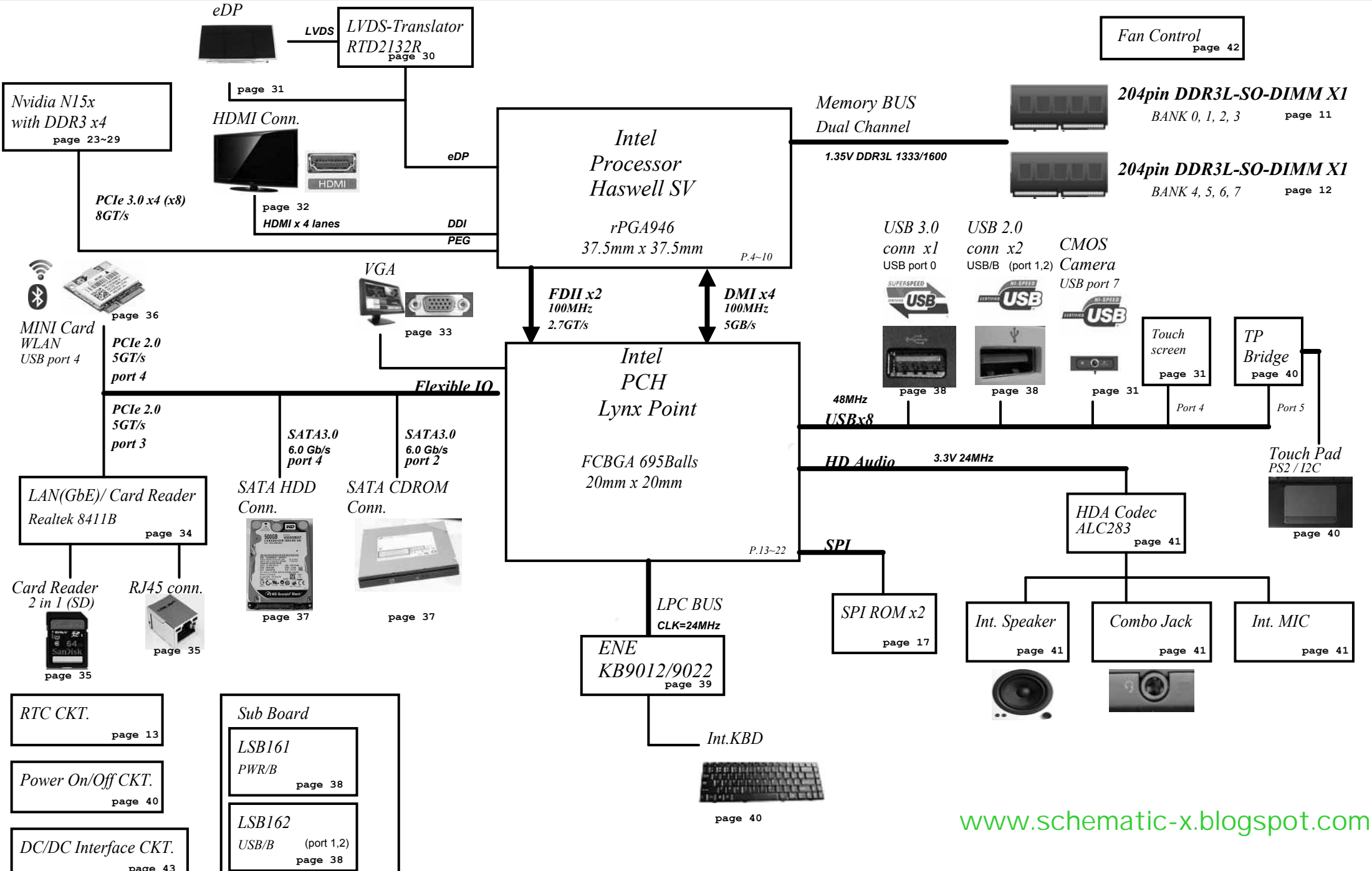
Nvidia N15S-GT / N15V-GM

2014-05-27

REV:1.0

DAX	
Part Number	Description
DAZ17F00100	PCB Z5WAW LA-B702P LS-B161P/B162P

Security Classification		Compal Secret Data		Title	
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Compal Electronics, Inc.	
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				Custom	Z5WAW M/B LA-B702
				Date	Tuesday, May 27, 2014
				Sheet	1 of 56
				Rev	0.2



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		Block Diagrams			
		Document Number	Z5WAW M/B LA-B702	Rev	0.2
		Date:	Tuesday, May 27, 2014	Sheet	2 of 56

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X	On Board Thermal Sensor	0100 110x
		VGA Internal Thermal Sensor	0100 000x

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA DIMM0	1010 0000 JDIMM1
ChannelB DIMM1	1010 0010 JDIMM2

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Finger Printer
	4	Touch Screen
	5	USB/I2C Bridge
	6	WLAN
	7	Webcam
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD
0	0	0 V	0 V	0 V	0x00-0x0B
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C-0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D-0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27-0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31-0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C-0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47-0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55-0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65-0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77-0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88-0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97-0xA3
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA4-0xAD
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xAE-0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8-0xC0
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC1-0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA-0xD3
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD4-0xDC
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDD-0xEE
19	NC	3.000 V	3.300 V		0xEE-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	-
3	0.3
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMAO@
GPU	VGA@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
DGPU_IDEN	VGM@, SGT@
VGM-820M;SGT-840M	
GC6 2.0	GC6@
non GC6	NGC6@
VRAM Selection	X76@
Digital MIC	1Dmic@/2Dmic@
USB/I2C BRI	TPBRI@
Touch Screen	TS@

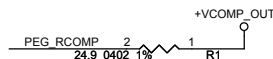
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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Notes List	
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				Z5WAW M/B LA-B702	0.2
				Date: Wednesday, May 28, 2014	Sheet 3 of 56

Haswell rPGA EDS
JCPU1A

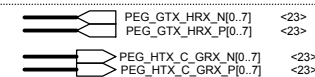
<14>	DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	D21	DMI_RXN_0
<14>	DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	C21	DMI_RXN_1
<14>	DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	B21	DMI_RXN_2
<14>	DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	A21	DMI_RXN_3
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<14>	DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	B20	DMI_RXP_2
<14>	DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	A20	DMI_RXP_3
<14>	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	D18	DMI_TXN_0
<14>	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	C17	DMI_TXN_1
<14>	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2	B17	DMI_TXN_2
<14>	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	A17	DMI_TXN_3
<14>	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	D17	DMI_TXP_0
<14>	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	C18	DMI_TXP_1
<14>	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	B18	DMI_TXP_2
<14>	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	A18	DMI_TXP_3

Design Guide show:
have to routed

<14>	FDI_CSXNC	FDI_CSXNC	H29	FDI_CSXNC
<14>	FDI_INT	FDI_INT	J29	DISP_INT



Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.

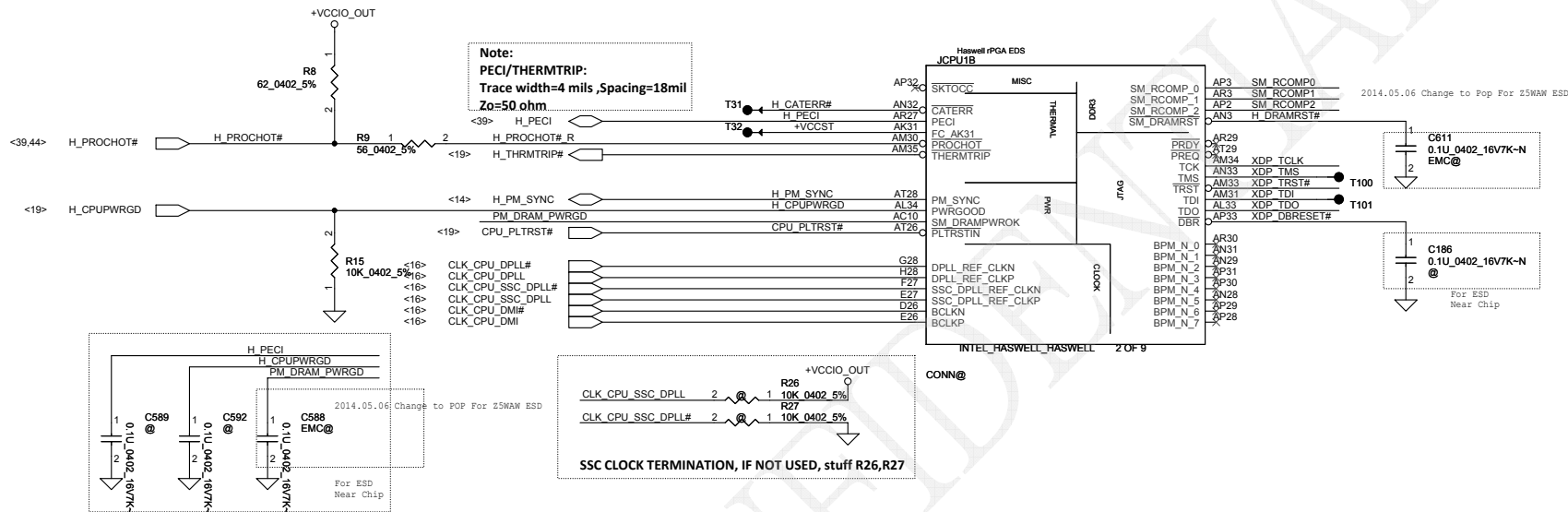


PEG_RCOMP	E23	PEG_RCOMP
PEG_RXN_0	M29	
PEG_RXN_1	K28	
PEG_RXN_2	J31	
PEG_RXN_3	I30	
PEG_RXN_4	H33	
PEG_RXN_5	G32	
PEG_RXN_6	F35	
PEG_RXN_7	E29	PEG GTX C HRX N7 0.22U 0402 10V6K VGM@ 2
PEG_RXN_8	D28	PEG GTX C HRX N6 0.22U 0402 10V6K VGM@ 2
PEG_RXN_9	E31	PEG GTX C HRX N5 0.22U 0402 10V6K VGM@ 2
PEG_RXN_10	D30	PEG GTX C HRX N4 0.22U 0402 10V6K VGM@ 2
PEG_RXN_11	E35	PEG GTX C HRX N3 0.22U 0402 10V6K VGM@ 2
PEG_RXN_12	D34	PEG GTX C HRX N2 0.22U 0402 10V6K VGM@ 2
PEG_RXN_13	E33	PEG GTX C HRX N1 0.22U 0402 10V6K VGM@ 2
PEG_RXN_14	E32	PEG GTX C HRX N0 0.22U 0402 10V6K VGM@ 2
PEG_RXN_15	L29	
PEG_RXP_0	L28	
PEG_RXP_1	L31	
PEG_RXP_2	K30	
PEG_RXP_3	J33	
PEG_RXP_4	I32	
PEG_RXP_5	H35	
PEG_RXP_6	G34	
PEG_RXP_7	F29	PEG GTX C HRX P7 0.22U 0402 10V6K VGM@ 2
PEG_RXP_8	E28	PEG GTX C HRX P6 0.22U 0402 10V6K VGM@ 2
PEG_RXP_9	F31	PEG GTX C HRX P5 0.22U 0402 10V6K VGM@ 2
PEG_RXP_10	E30	PEG GTX C HRX P4 0.22U 0402 10V6K VGM@ 2
PEG_RXP_11	F36	PEG GTX C HRX P3 0.22U 0402 10V6K VGM@ 2
PEG_RXP_12	E34	PEG GTX C HRX P2 0.22U 0402 10V6K VGM@ 2
PEG_RXP_13	F33	PEG GTX C HRX P1 0.22U 0402 10V6K VGM@ 2
PEG_RXP_14	D32	PEG GTX C HRX P0 0.22U 0402 10V6K VGM@ 2
PEG_TXN_0	H35	
PEG_TXN_1	I34	
PEG_TXN_2	J33	
PEG_TXN_3	K32	
PEG_TXN_4	L30	
PEG_TXN_5	M33	
PEG_TXN_6	N32	
PEG_TXN_7	B31	PEG HTX GRX N7 0.22U 0402 10V6K VGM@ 2
PEG_TXN_8	A30	PEG HTX GRX N6 0.22U 0402 10V6K VGM@ 2
PEG_TXN_9	B29	PEG HTX GRX N5 0.22U 0402 10V6K VGM@ 2
PEG_TXN_10	A28	PEG HTX GRX N4 0.22U 0402 10V6K VGM@ 2
PEG_TXN_11	B27	PEG HTX GRX N3 0.22U 0402 10V6K VGM@ 2
PEG_TXN_12	A26	PEG HTX GRX N2 0.22U 0402 10V6K VGM@ 2
PEG_TXN_13	B25	PEG HTX GRX N1 0.22U 0402 10V6K VGM@ 2
PEG_TXN_14	A24	PEG HTX GRX N0 0.22U 0402 10V6K VGM@ 2
PEG_TXN_15	J35	
PEG_TXP_0	K34	
PEG_TXP_1	L33	
PEG_TXP_2	M32	
PEG_TXP_3	N30	
PEG_TXP_4	O31	
PEG_TXP_5	P30	
PEG_TXP_6	Q33	
PEG_TXP_7	R32	
PEG_TXP_8	C31	PEG HTX GRX P7 0.22U 0402 10V6K VGM@ 2
PEG_TXP_9	B30	PEG HTX GRX P6 0.22U 0402 10V6K VGM@ 2
PEG_TXP_10	C29	PEG HTX GRX P5 0.22U 0402 10V6K VGM@ 2
PEG_TXP_11	B28	PEG HTX GRX P4 0.22U 0402 10V6K VGM@ 2
PEG_TXP_12	C27	PEG HTX GRX P3 0.22U 0402 10V6K VGM@ 2
PEG_TXP_13	B26	PEG HTX GRX P2 0.22U 0402 10V6K VGM@ 2
PEG_TXP_14	C25	PEG HTX GRX P1 0.22U 0402 10V6K VGM@ 2
PEG_TXP_15	B24	PEG HTX GRX P0 0.22U 0402 10V6K VGM@ 2

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CONN@

1 OF 9

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Issued Date	2013/12/26	Deciphered Date	2014/12/26	PROCESSOR(1/7) DMI,FDI,PEG	
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				Date: Tuesday, May 27, 2014	Sheet 4 of 56

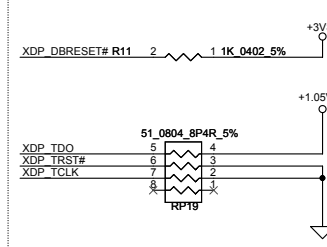


DDR3 COMPENSATION SIGNALS

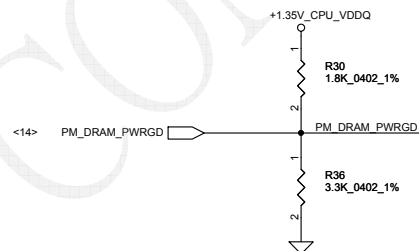
SM_RCOMP0R5	1	2	100_0402_1%
SM_RCOMP1R6	1	2	75_0402_1%
SM_RCOMP2R7	1	2	100_0402_1%

Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mils

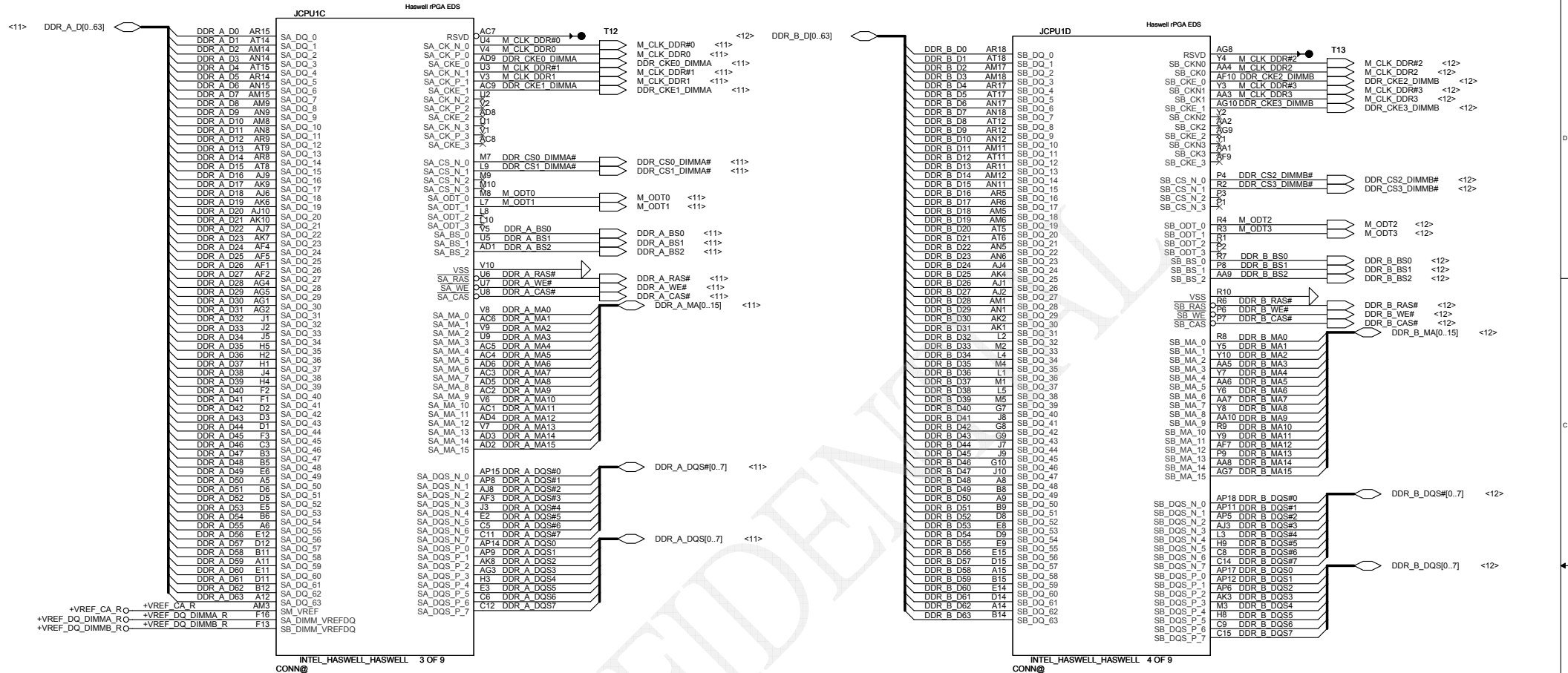
PU/PD for JTAG signals



SM_DRAMPWROK with DDR Power Gating Topology



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		Date	Tuesday, May 27, 2014
		Rev	0.2
		Sheet	5 of 56



HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

<32> HDMI_TX2-
<32> HDMI_TX2+
<32> HDMI_TX1-
<32> HDMI_TX1+
<32> HDMI_TX0-
<32> HDMI_TX0+
<32> HDMI_CLK-
<32> HDMI_CLK+

HDMI_TX2- 0.1U 0402 16V7K 1
HDMI_TX2+ 0.1U 0402 16V7K 1
HDMI_TX1- 0.1U 0402 16V7K 1
HDMI_TX1+ 0.1U 0402 16V7K 1
HDMI_TX0- 0.1U 0402 16V7K 1
HDMI_TX0+ 0.1U 0402 16V7K 1
HDMI_CLK- 0.1U 0402 16V7K 1
HDMI_CLK+ 0.1U 0402 16V7K 1

2 C410 CPU DP2 N0
2 C400 CPU DP2 P0
2 C395 CPU DP2 N1
2 C409 CPU DP2 P1
2 C408 CPU DP2 N2
2 C406 CPU DP2 P2
2 C412 CPU DP2 N3
2 C411 GPU DP2 P3

T28
U28
T30
U30
U29
V29
U31
V31

Haswell iPGA EDS

JCPU1H

DDIB_TXBN_0
DDIB_TXBP_0
DDIB_TXBN_1
DDIB_TXBP_1
DDIB_TXBN_2
DDIB_TXBP_2
DDIB_TXBN_3
DDIB_TXBP_3

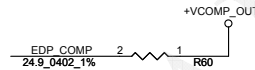
DDIC_TXCN_0
DDIC_TXCP_0
DDIC_TXCN_1
DDIC_TXCP_1
DDIC_TXCN_2
DDIC_TXCP_2
DDIC_TXCN_3
DDIC_TXCP_3

DDID_TXDN_0
DDID_TXDP_0
DDID_TXDN_1
DDID_TXDP_1
DDID_TXDN_2
DDID_TXDP_2
DDID_TXDN_3
DDID_TXDP_3

CONN@

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COMPENSATION PU FOR eDP



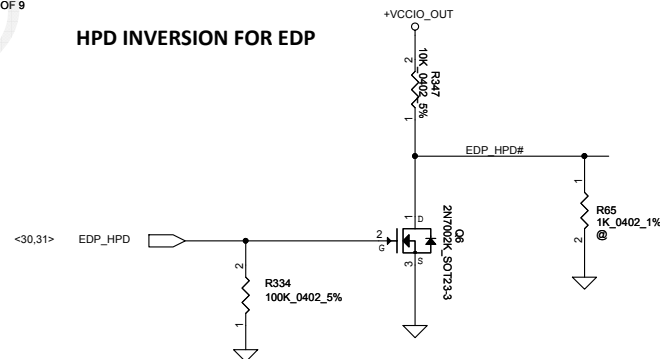
Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

EDP_AUXN
EDP_AUXP
EDP_HPDI
EDP_RCOMP
EDP_DISP_UT IL

EDP_TXN_0
EDP_TXP_0
EDP_TXN_1
EDP_TXP_1
FDI_TXN_0
FDI_TXP_0
FDI_TXN_1
FDI_TXP_1

DDI

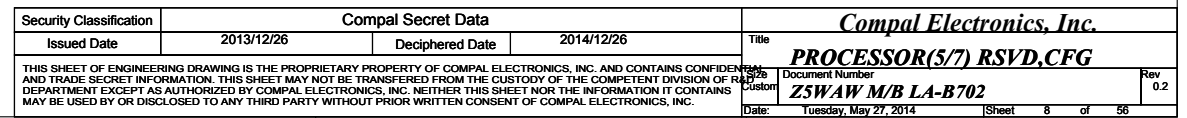
HPD INVERSION FOR EDP



HPD is a active high signal from device.
The HPD processor input is a low voltage
active signal.

A schematic diagram showing a resistor labeled R62 with a value of 1K_0402_1% connected to the CFG2 pin. The resistor is represented by a zigzag line between pin 1 and pin 2. Pin 1 is connected to the CFG2 signal line, and pin 2 is connected to ground, indicated by a triangle symbol.

PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



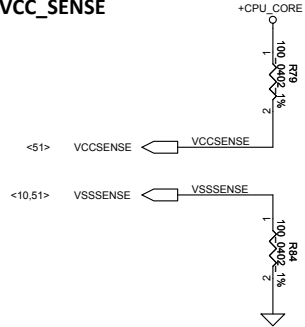


Figure 10. Schematic diagram of the CPU power supply circuit

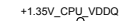
Place to TOP CPU socket cavity

Diagram showing the placement of capacitors C140, C141, C142, and C257 on the TOP CPU socket cavity. The capacitors are connected to the CPU pins 10L_0603_6.3V6M-N and 10L_0603_6.3V6M-N. The diagram shows the capacitors connected to the CPU pins and the ground plane.

```
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<51> VR_SVID_CLK
<51> VR_SVID_DAT
```

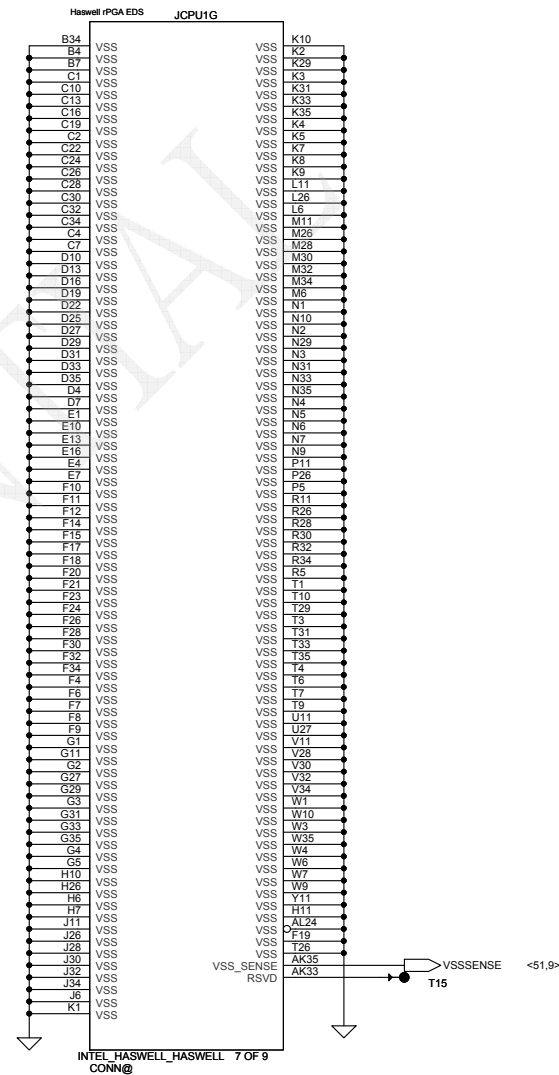
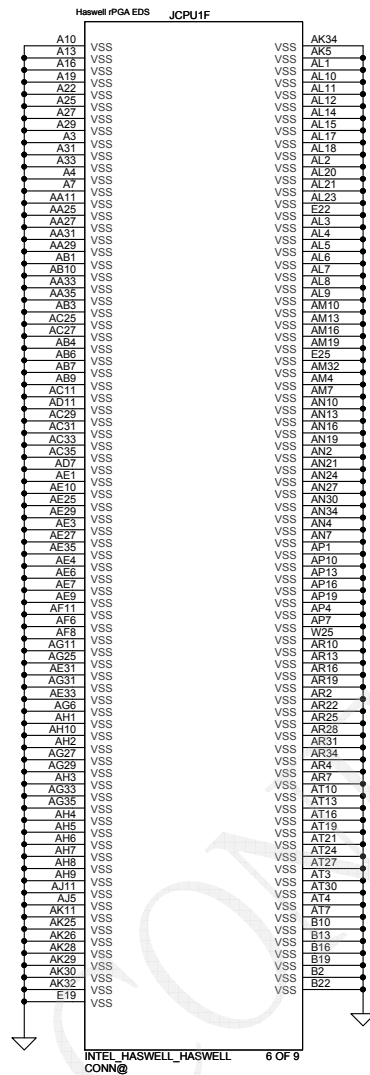
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<51> VR_SVID_CLK
<51> VR_SVID_DAT
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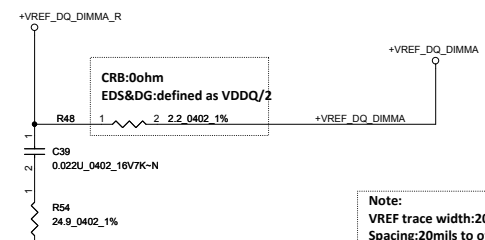
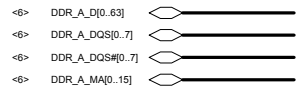
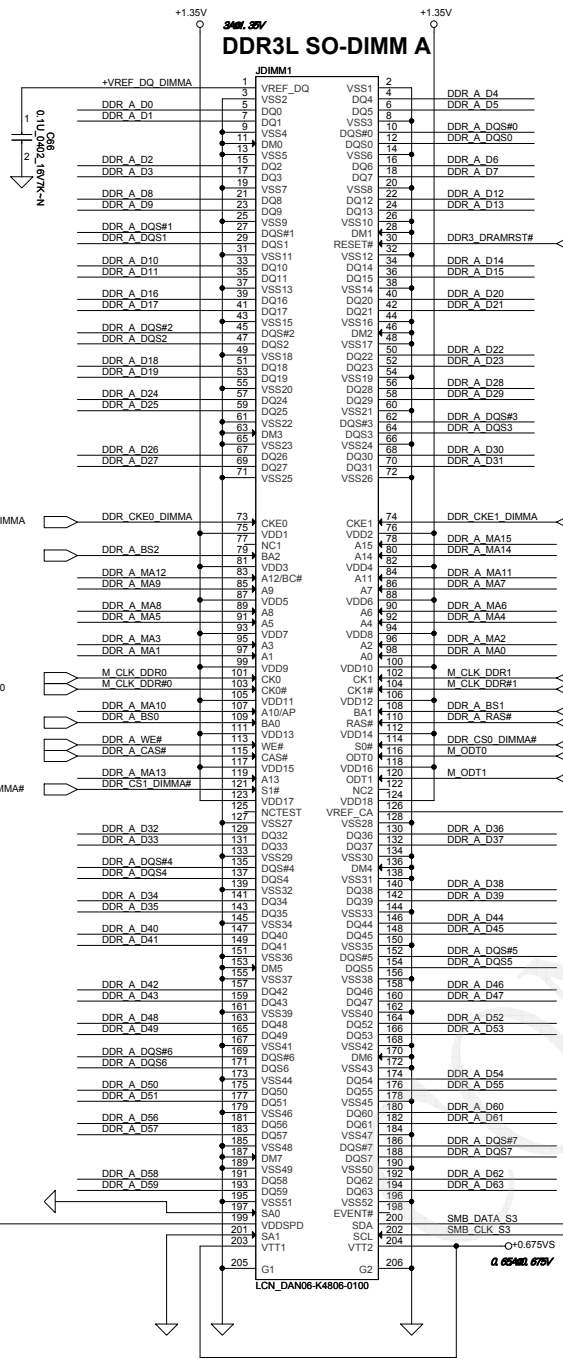
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<51> VR_SVID_ALRT#
<51> VR_SVID_CLK
<51> VR_SVID_DAT
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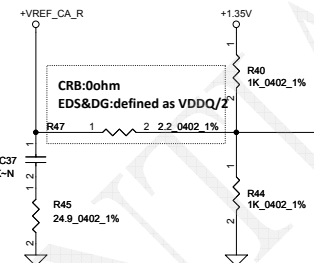
Haswell iPGA EDS	JCPU1E	+CPU_CORE
	VCC	AA26
	VCC	AA28
	VCC	AA34
RSVD	VCC	AA30
RSVD	VCC	AA32
RSVD	VCC	AB26
RSVD	VCC	AB29
	VCC	AB25
	VCC	AB27
	VCC	AB28
	VCC	AB30
VDDQ	VCC	AB31
VDDQ	VCC	AB33
VDDQ	VCC	AB34
VDDQ	VCC	AB32
VDDQ	VCC	AC28
VDDQ	VCC	AC29
VDDQ	VCC	AC32
VDDQ	VCC	AC33
VDDQ	VCC	AC30
VDDQ	VCC	AD28
VDDQ	VCC	AD32
VDDQ	VCC	AD31
VDDQ	VCC	AD34
VDDQ	VCC	AD26
VDDQ	VCC	AD27
VDDQ	VCC	AD29
VDDQ	VCC	AD30
VDDQ	VCC	AD32
VDDQ	VCC	AD33
VDDQ	VCC	AD35
RSVD	VCC	AE26
VCC	VCC	AE32
RSVD	VCC	AE28
RSVD	VCC	AE30
	VCC	AG28
	VCC	AG34
	VCC	AF34
	VCC	AF25
	VCC	AF26
	VCC	AF27
VCC_SENSE	VCC	AF28
RSVD	VCC	AF29
VCCIO_OUT	VCC	AF30
RSVD	VCC	AF31
VCOMP_OUT	VCC	AF32
RSVD	VCC	AF33
RSVD	VCC	AF34
RSVD	VCC	AF35
RSVD	VCC	AG26
	VCC	AH26
	VCC	AH29
VIDALERT	VCC	AG30
VIDSCOUT	VCC	AG32
	VCC	AH32
	VCC	AH35
VSS	VCC	AH25
PWR_DEBUG	VCC	AH27
VSS	VCC	AH28
RSVD_TP	VCC	AH30
RSVD_TP	VCC	AH31
RSVD_TP	VCC	AH33
RSVD_TP	VCC	AH34
VSS	VCC	AJ25
VSS	VCC	AJ26
VSS	VCC	AJ27
VSS	VCC	AJ28
VSS	VCC	AJ29
VSS	VCC	AJ30
VSS	VCC	AJ31
VSS	VCC	AJ32
VSS	VCC	AJ33
VSS	VCC	AJ34
VSS	VCC	AJ35
VSS	VCC	G25
VSS	VCC	H25
VSS	VCC	J25
VSS	VCC	K25
VSS	VCC	L25
VSS	VCC	M25
VCC	VCC	N25
VCC	VCC	P25
VCC	VCC	R25
VCC	VCC	T25
VCC	VCC	U25
VCC	VCC	U26
VCC	VCC	V25
VCC	VCC	V26
VCC	VCC	W26
VCC	VCC	W27

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				Size	
				Custom	
				Document Number	Rev
				Z5WAW M/B LA-B702	0.2
Date:				Tuesday, May 27, 2014	Sheet 9 of 56

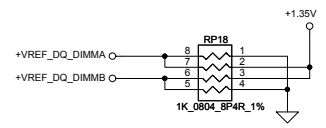




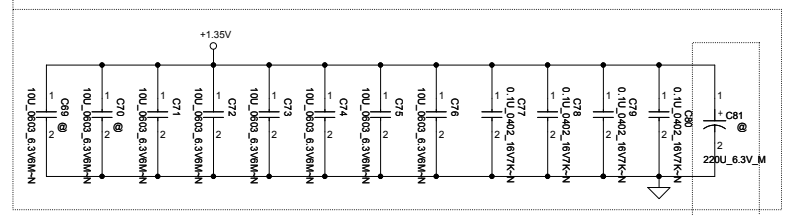
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket



Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

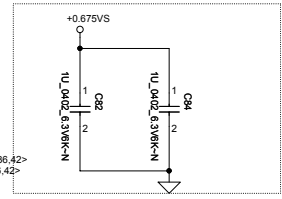


Layout Note:
Place near DIMM



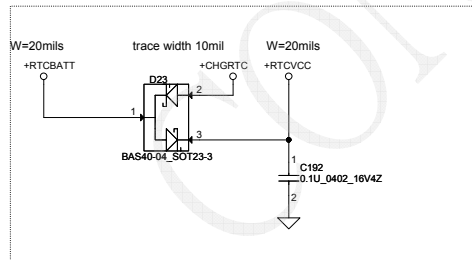
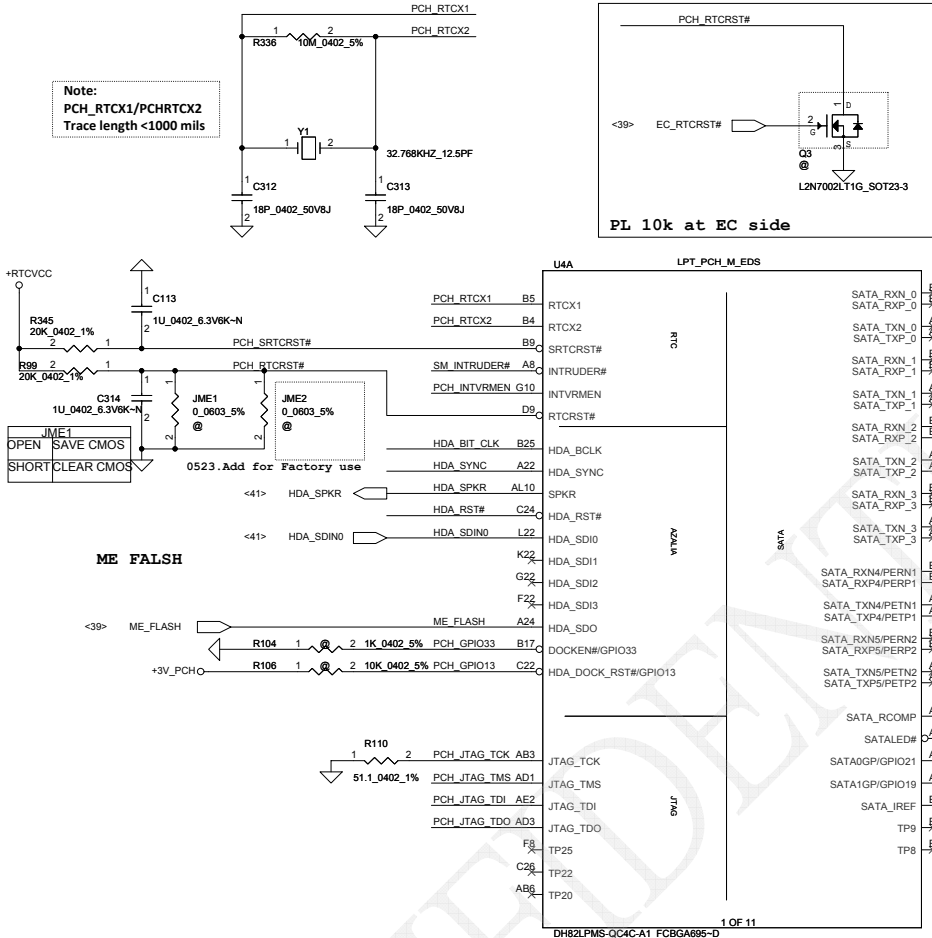
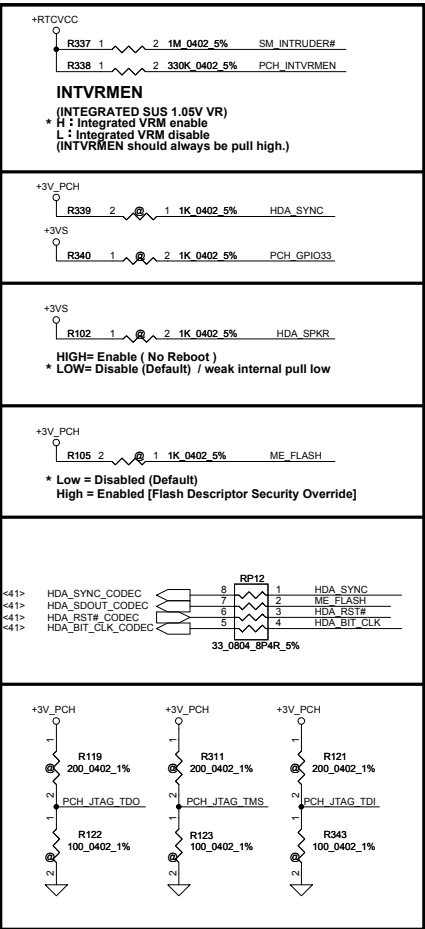
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220U 6.3V OSCON
ESR 17mohm@100Khz

Layout Note:
Place near DIMM

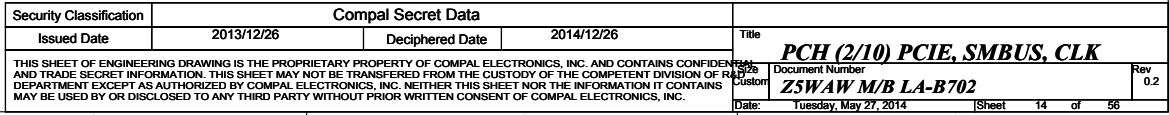


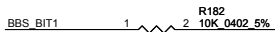
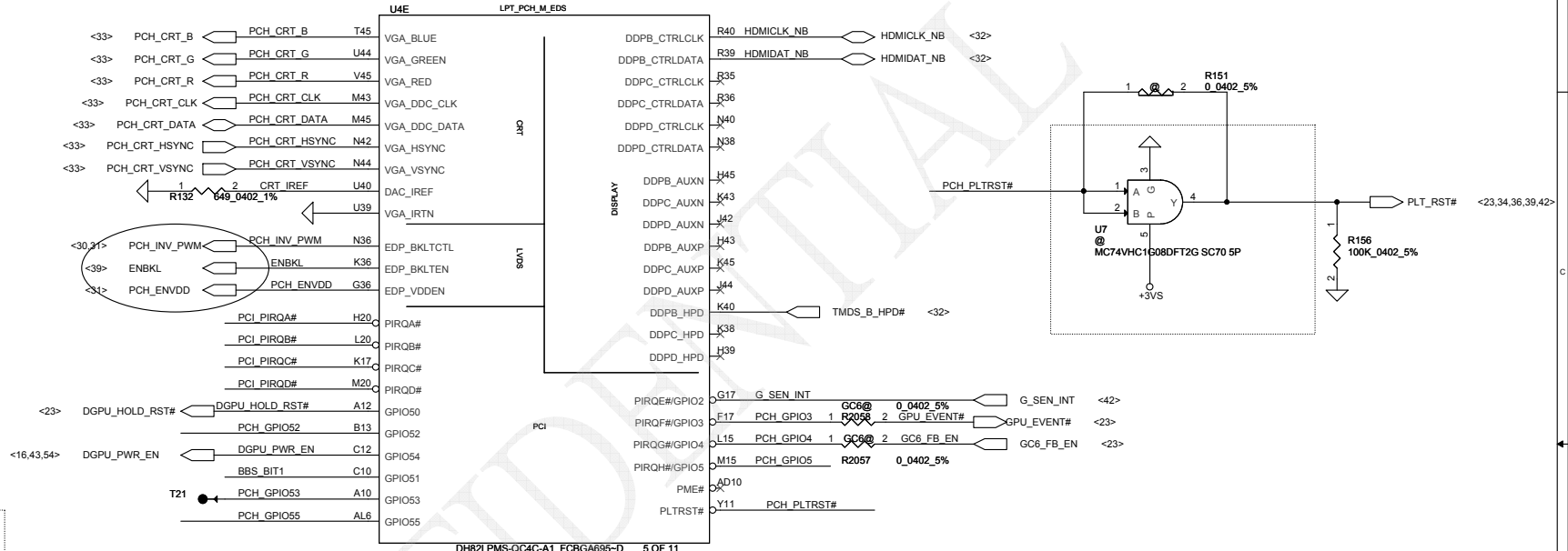
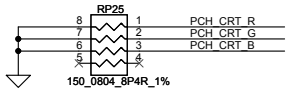
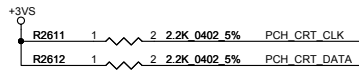
DIMM_A STD H:8mm
<Address: 00>
SP07000N400

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				Date	Tuesday, May 27, 2014
				Sheet	11 of 58



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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	PCH (1/10) SATA,HDA,SPI, LPC, XDP
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				Date	Tuesday, May 27, 2014
				Sheet	13 of 56

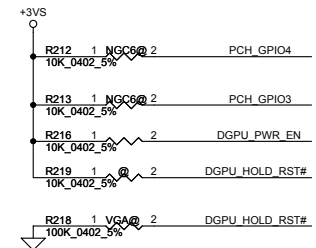
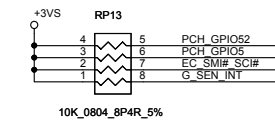
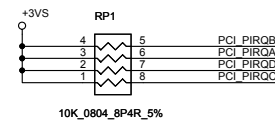
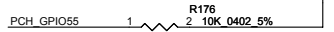
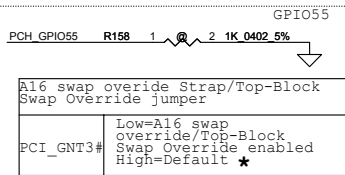




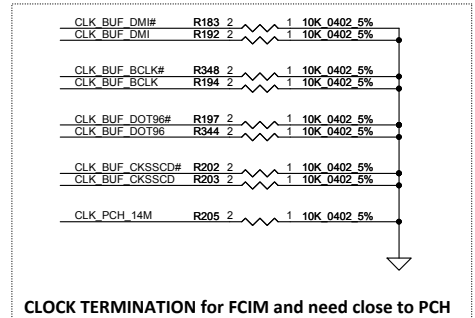
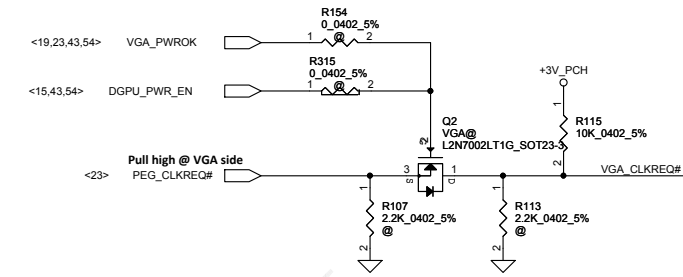
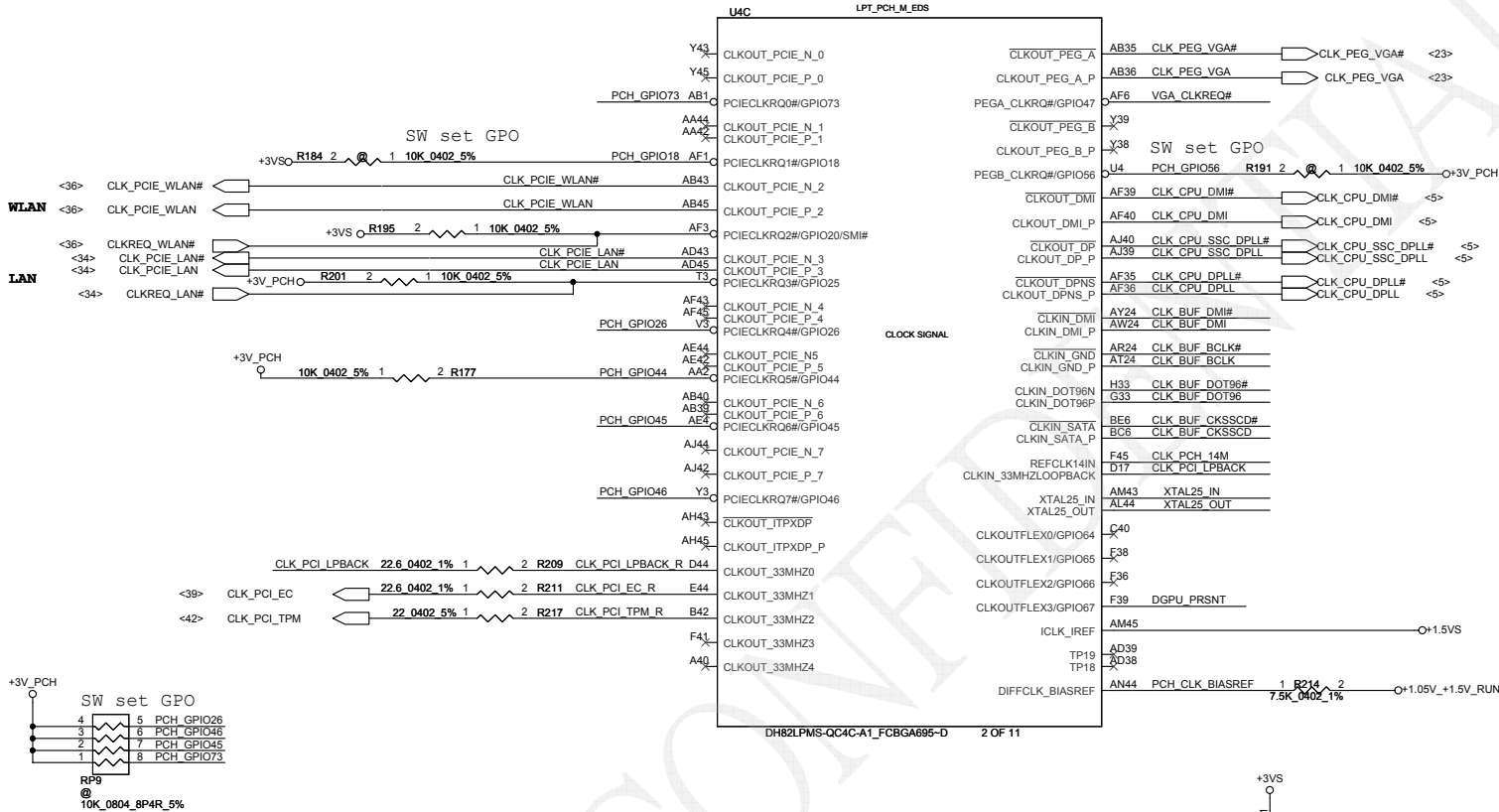
Boot BIOS Strap (GPIO51)

BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

GPIO51 has internal pull up.

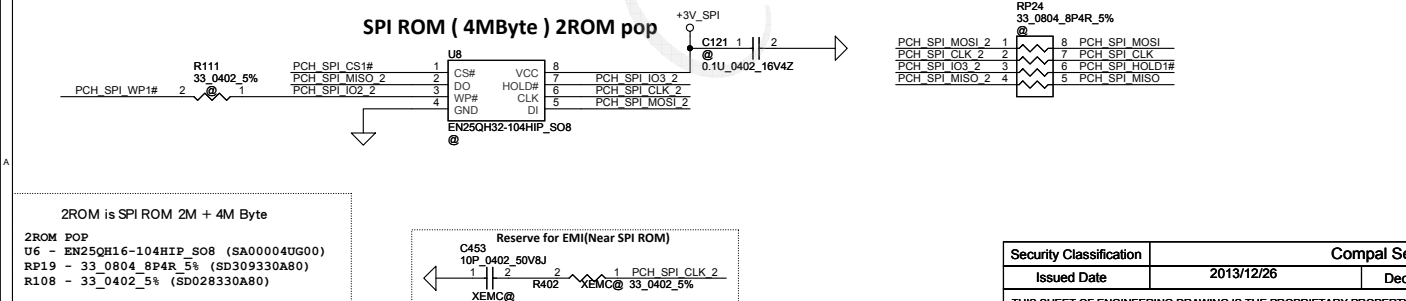
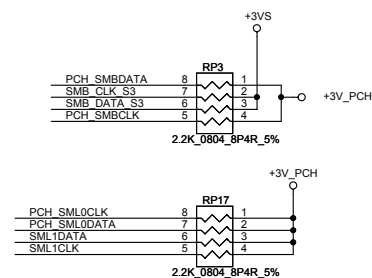
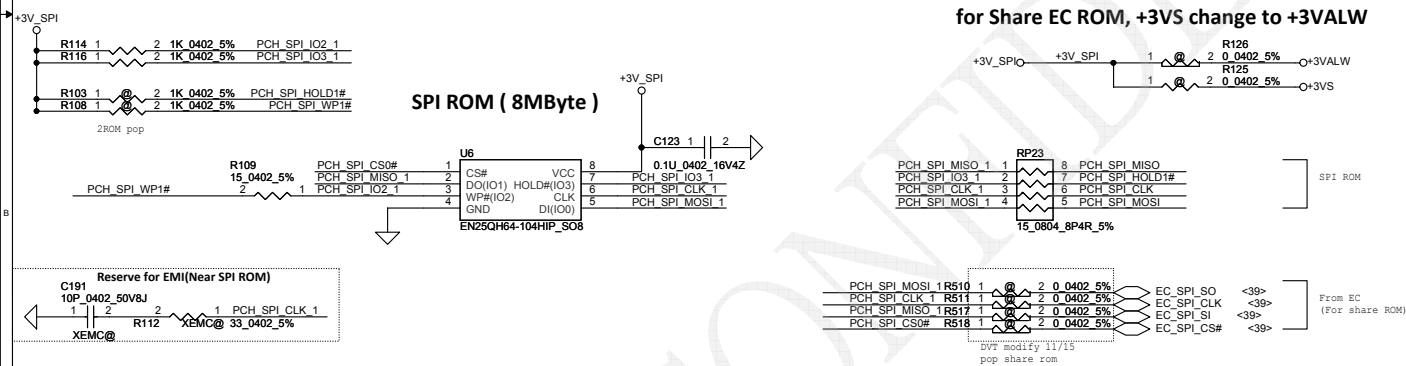
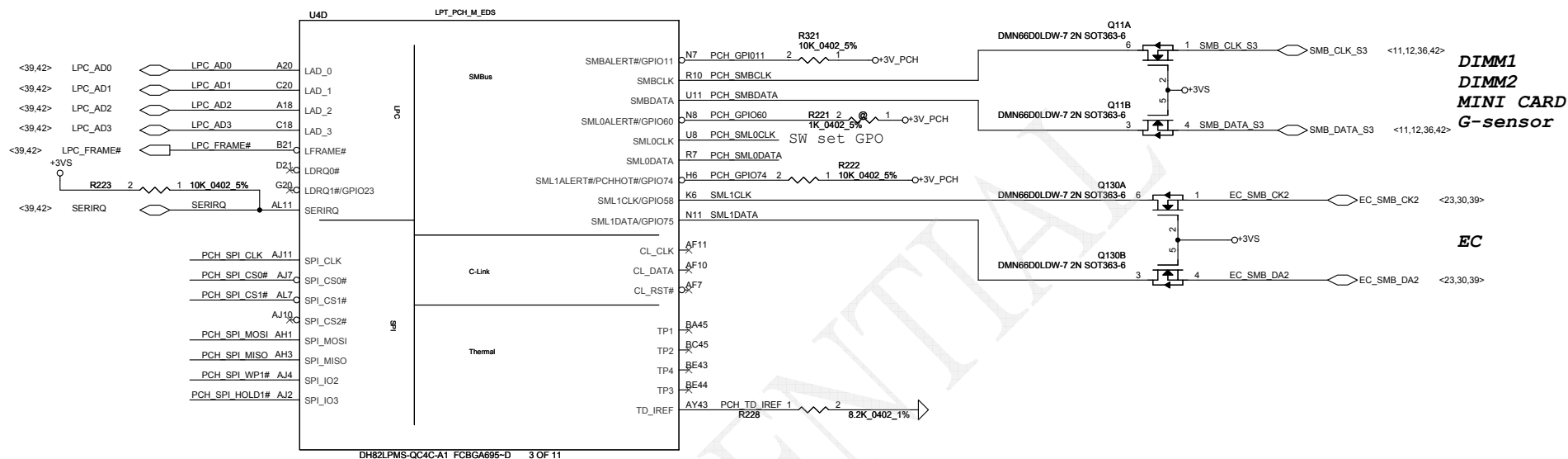


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				Document Number		Z5WAW M/B LA-B702	
				Date		Tuesday, May 27, 2014	
				Sheet		15 of 56	
				Rev		0.2	

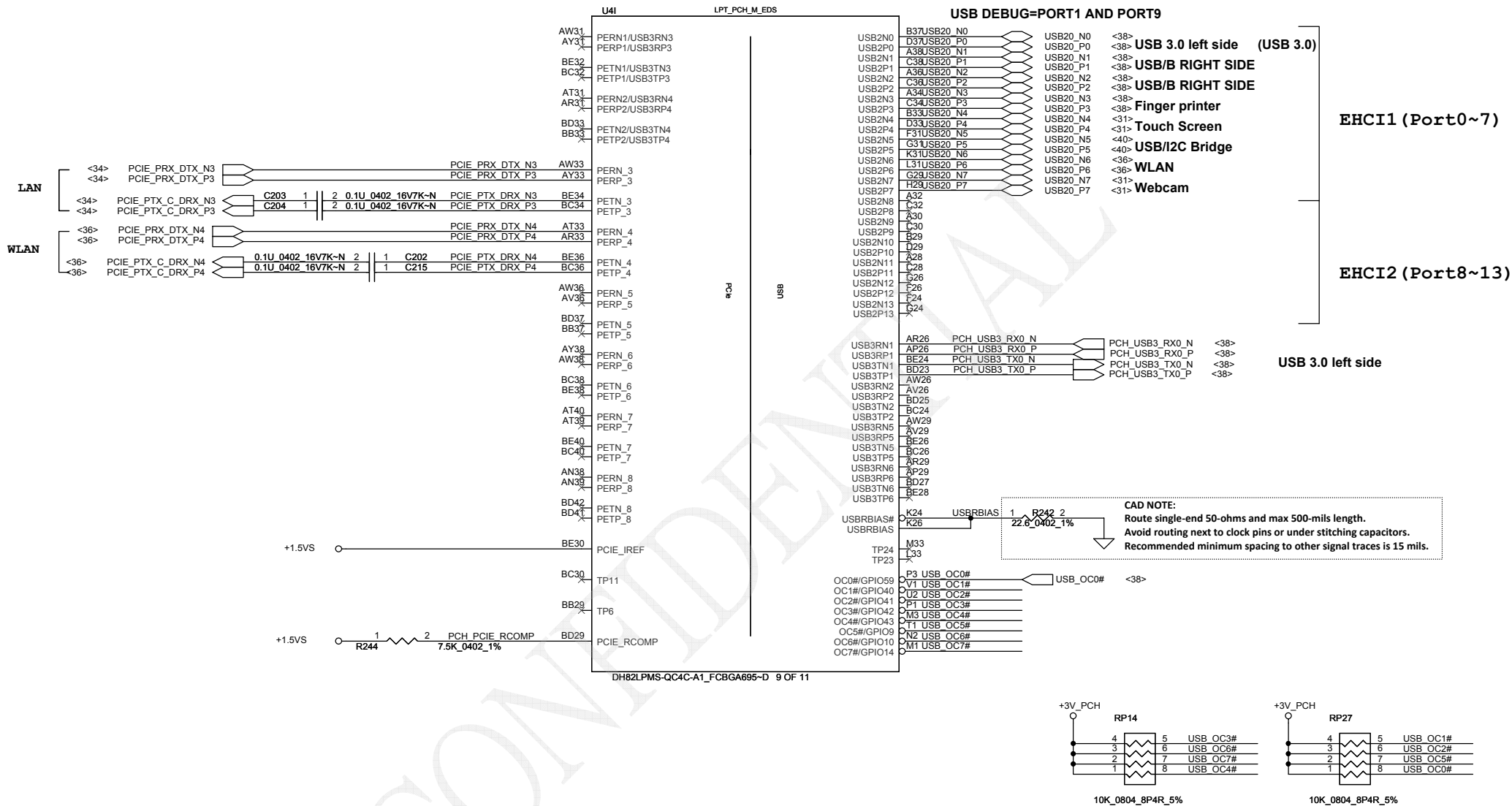


CLOCK TERMINATION for FCIM and need close to PCH

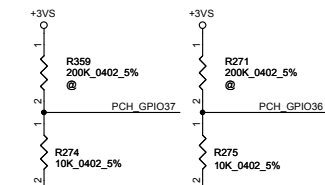
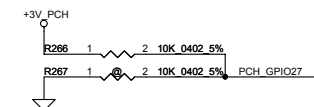
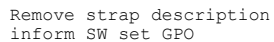
DGPU_PRSNT	Function
0	UMA
1	Optimus



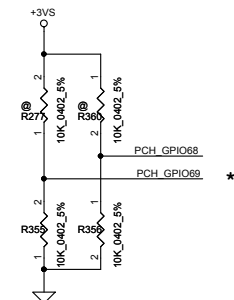
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	PCH (5/10) LVDS,CRT,DP,HDMI	
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				Custom	Z5WAW M/B LA-B702	
Date: Tuesday, May 27, 2014				Sheet	17	of 56



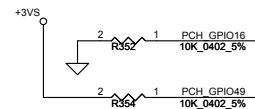
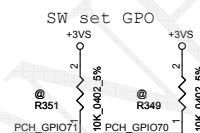
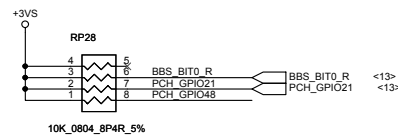
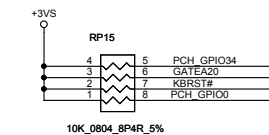
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Issued Date	2013/12/26	Deciphered Date	2014/12/26		
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					Document Number
					Customer
					Rev 0.2
					Date: Tuesday, May 27, 2014
					Sheet 18 of 56



BIOS Request SKU ID

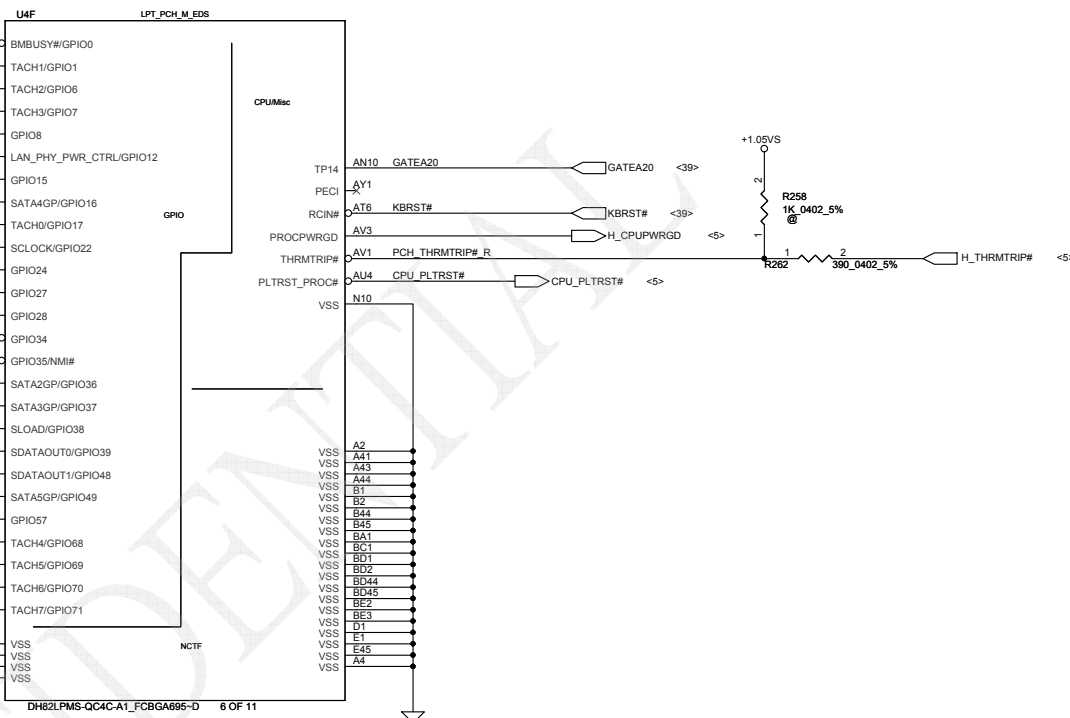


PCH_GPIO68	PCH_GPIO69	Function
0	0	Z5WAW
0	1	Reserved
1	0	Reserved
1	1	Reserved

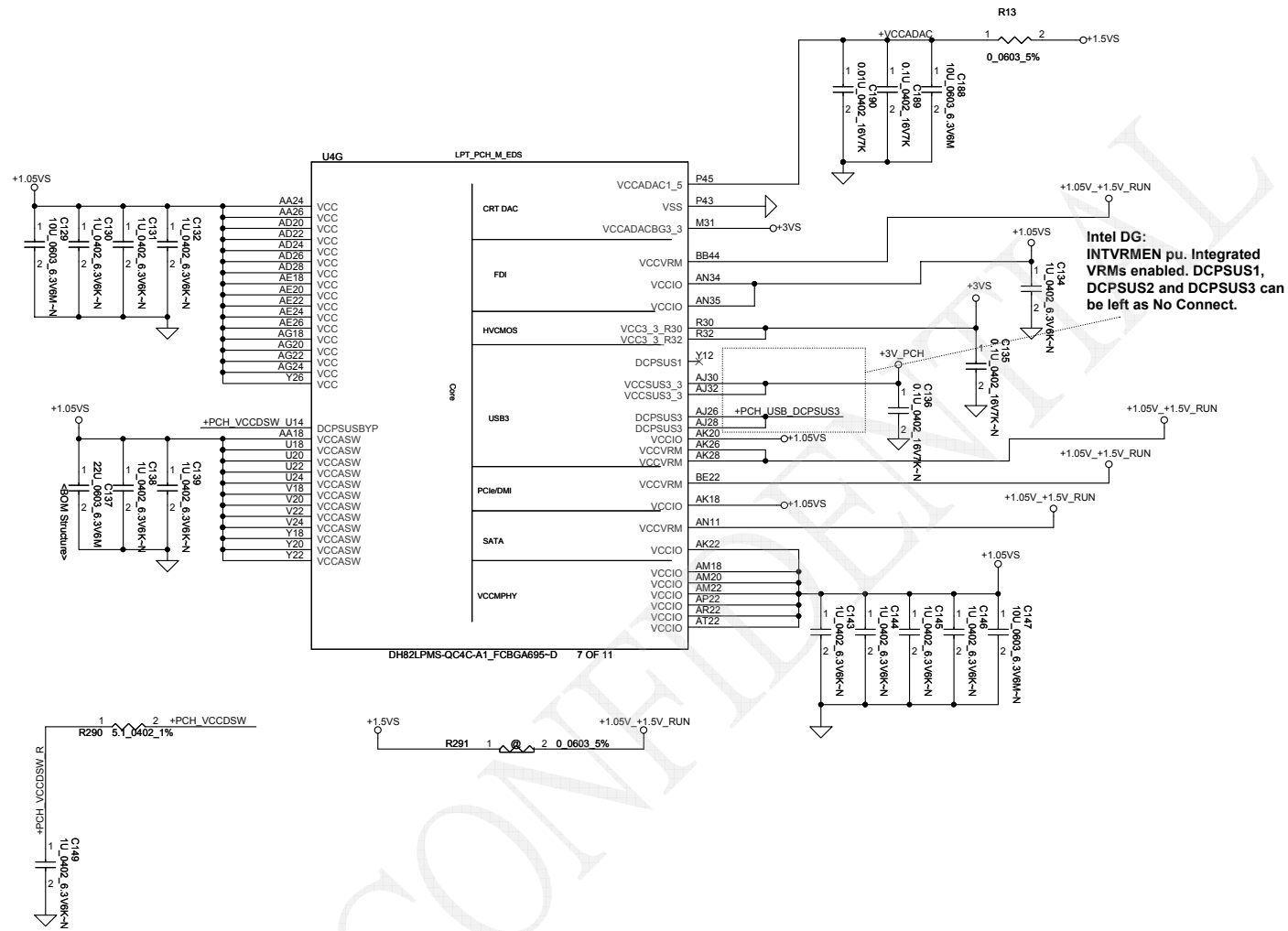


	Config	GPIO16 & 49
	USB3.0 x4, PCIE x8, SATA x6	11
*	USB3.0 x6, PCIE x8, SATA x4	01

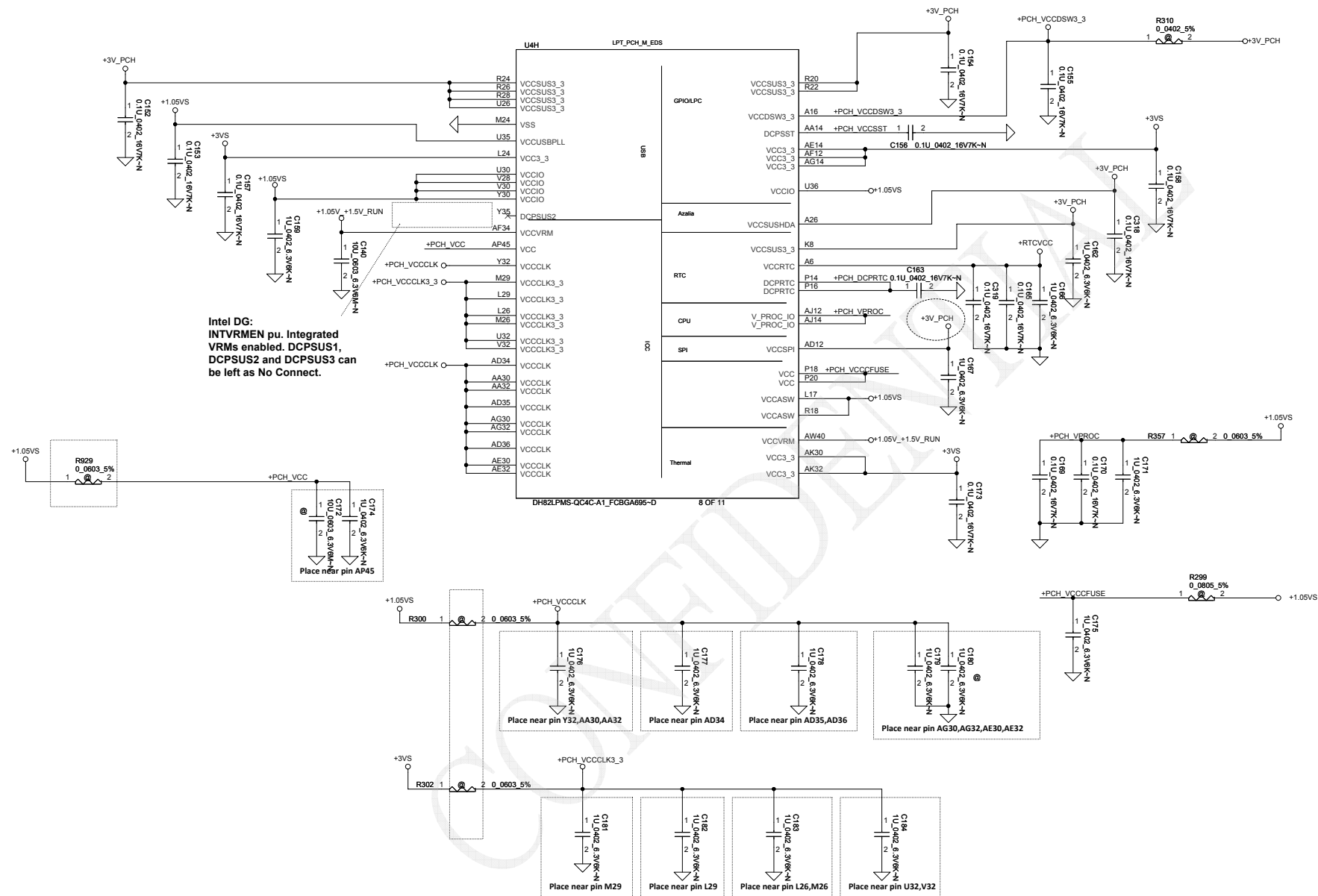
Fixed Signals				Fixed Signals		Fixed Signals				Fixed Signals		Fixed Signals					
Fixed Signals				Fixed Signals		Fixed Signals				Fixed Signals		Fixed Signals					
US03_1	US03_2	US03_3	US03_4	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3
				(00)	(00)												
				US03_3	US03_4												
				(01)	(01)												



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				Document Number ZSWAW M/B LA-B702		
Date: Tuesday, May 27 2014				ISheet 10 of 56		

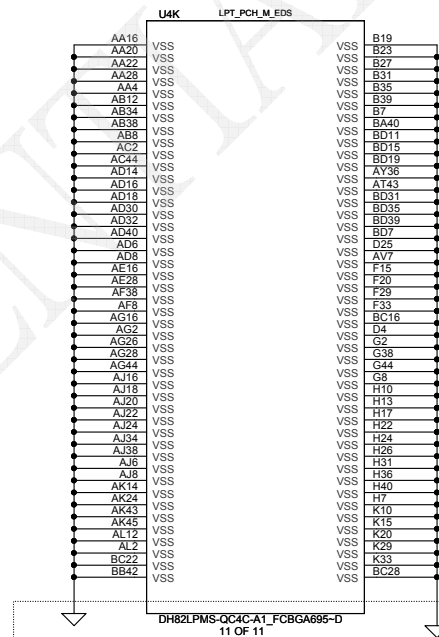
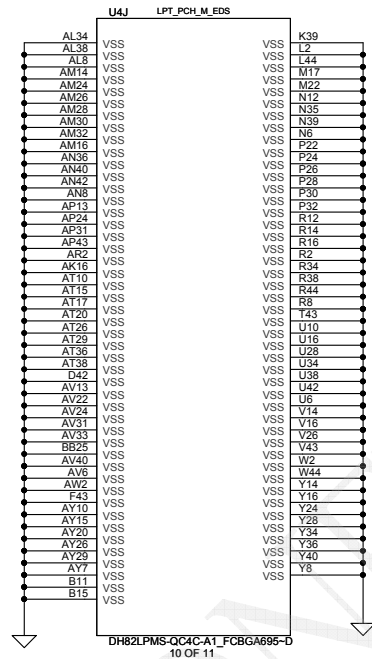


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

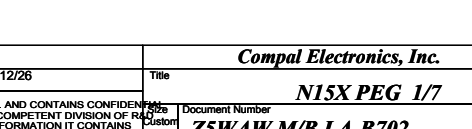
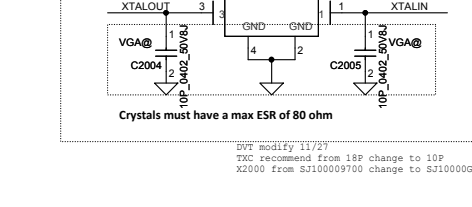
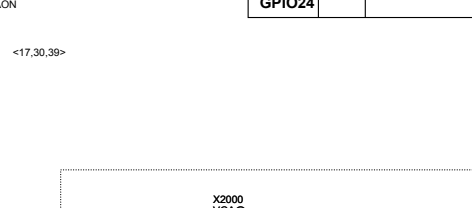
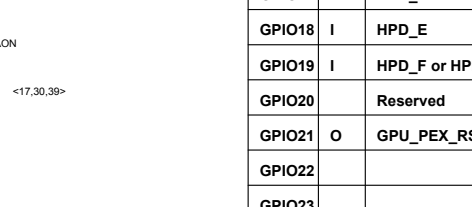
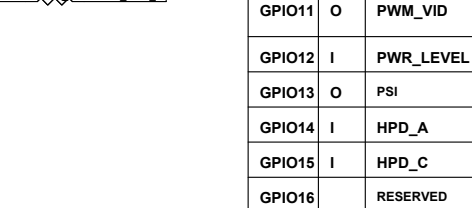
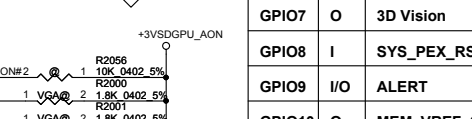
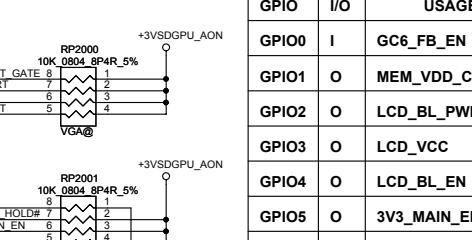
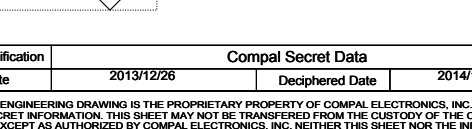
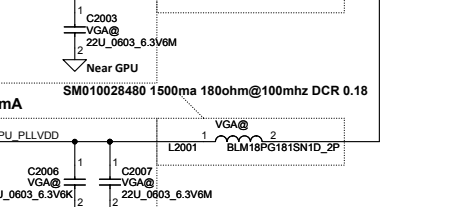
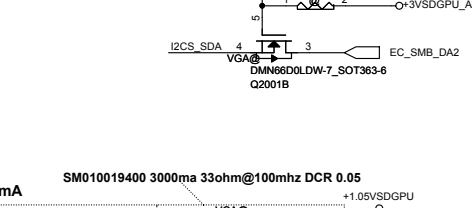
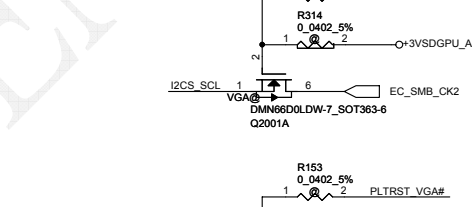
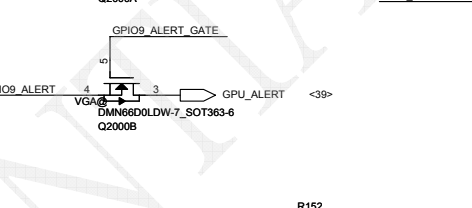
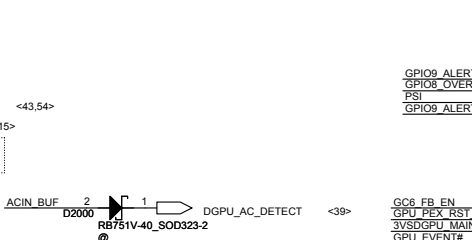
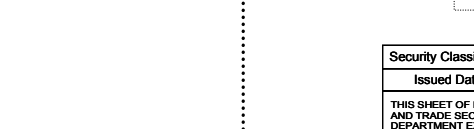
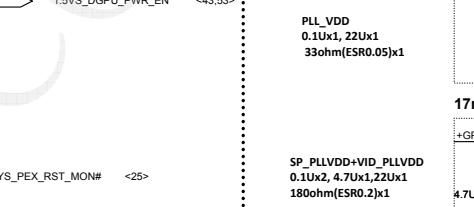
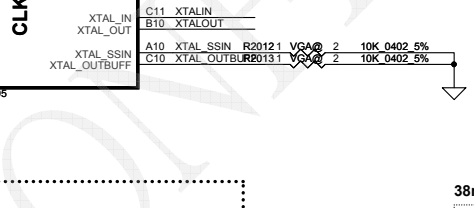
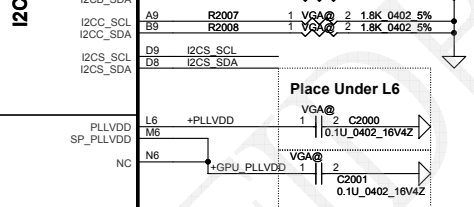
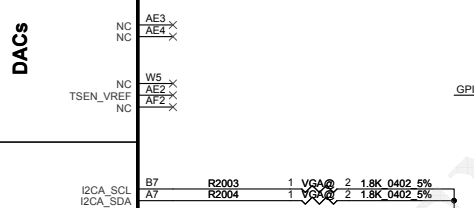
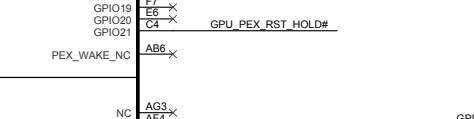
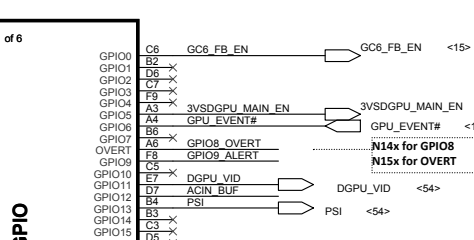
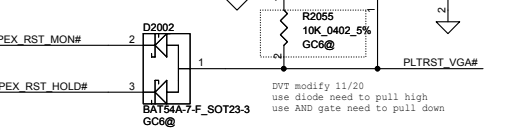
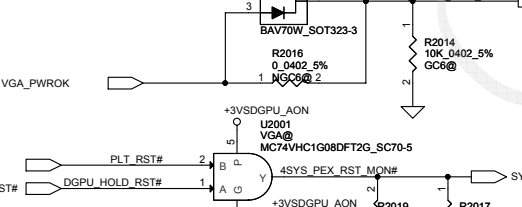
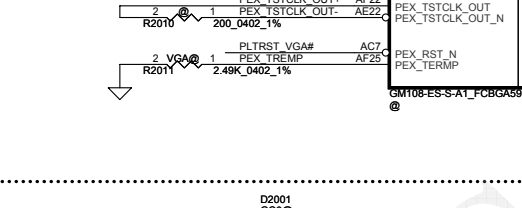
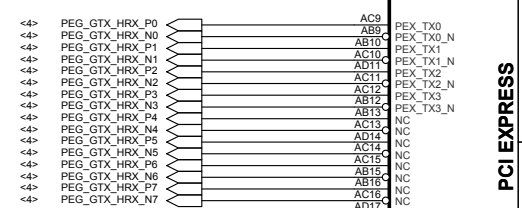
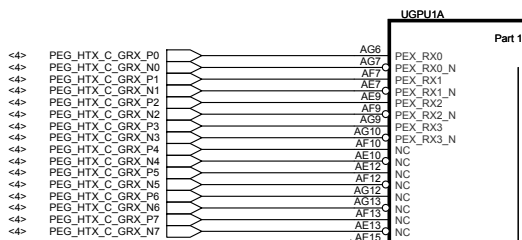


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

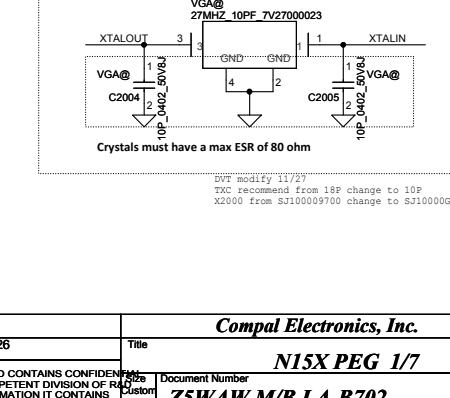
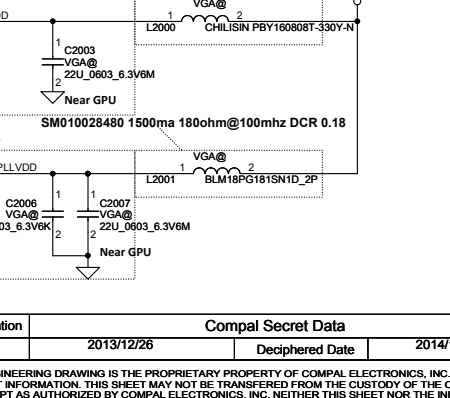
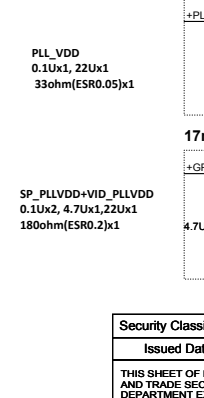
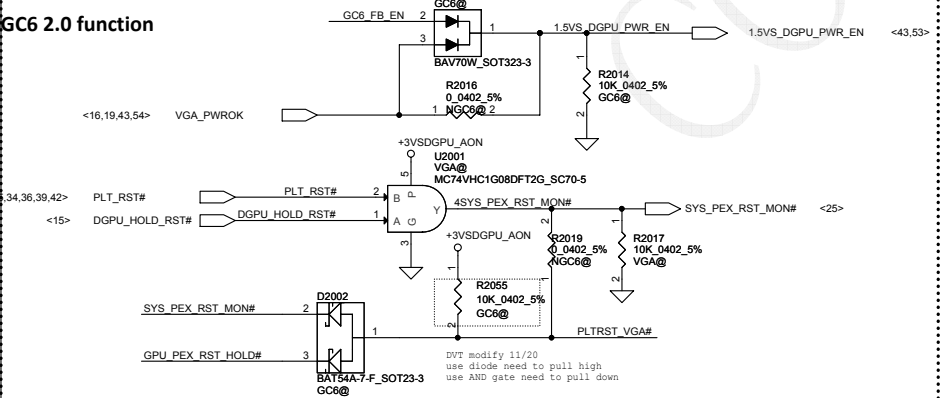
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Date: Tuesday, May 27, 2014				Document Number Z5WAW M/B LA-B702	Sheet 21 of 58



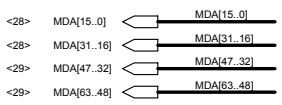
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				Z5WAW M/B LA-B702		0.2	
				Date:	Tuesday, May 27, 2014	Sheet	22 of 56



GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

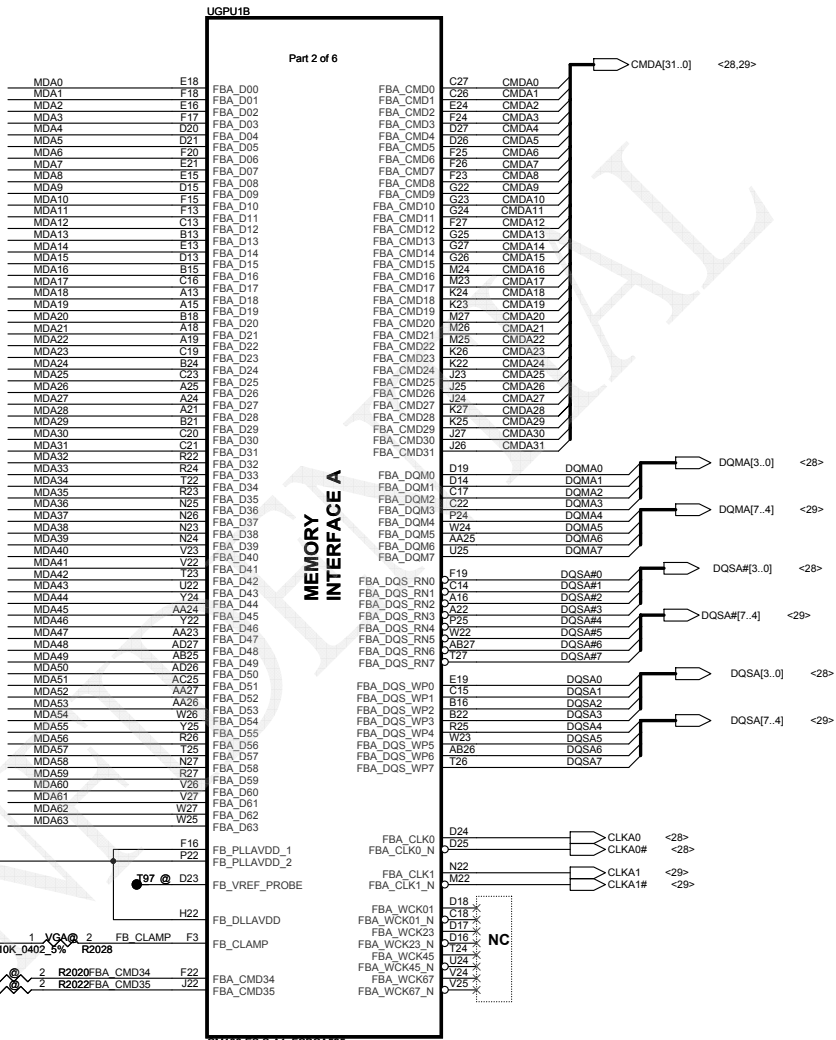
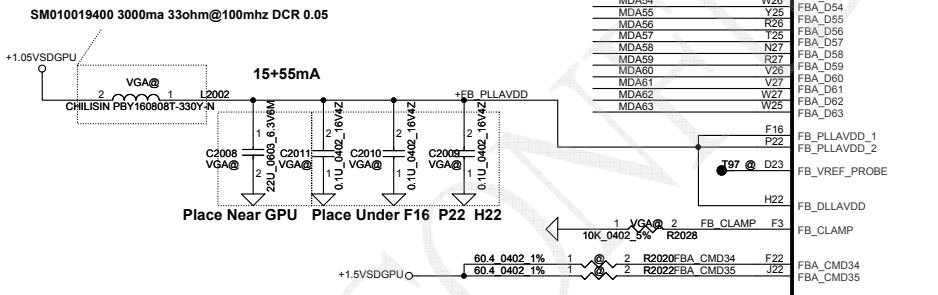


VRAM Interface



NV 15x DG-06803-V03

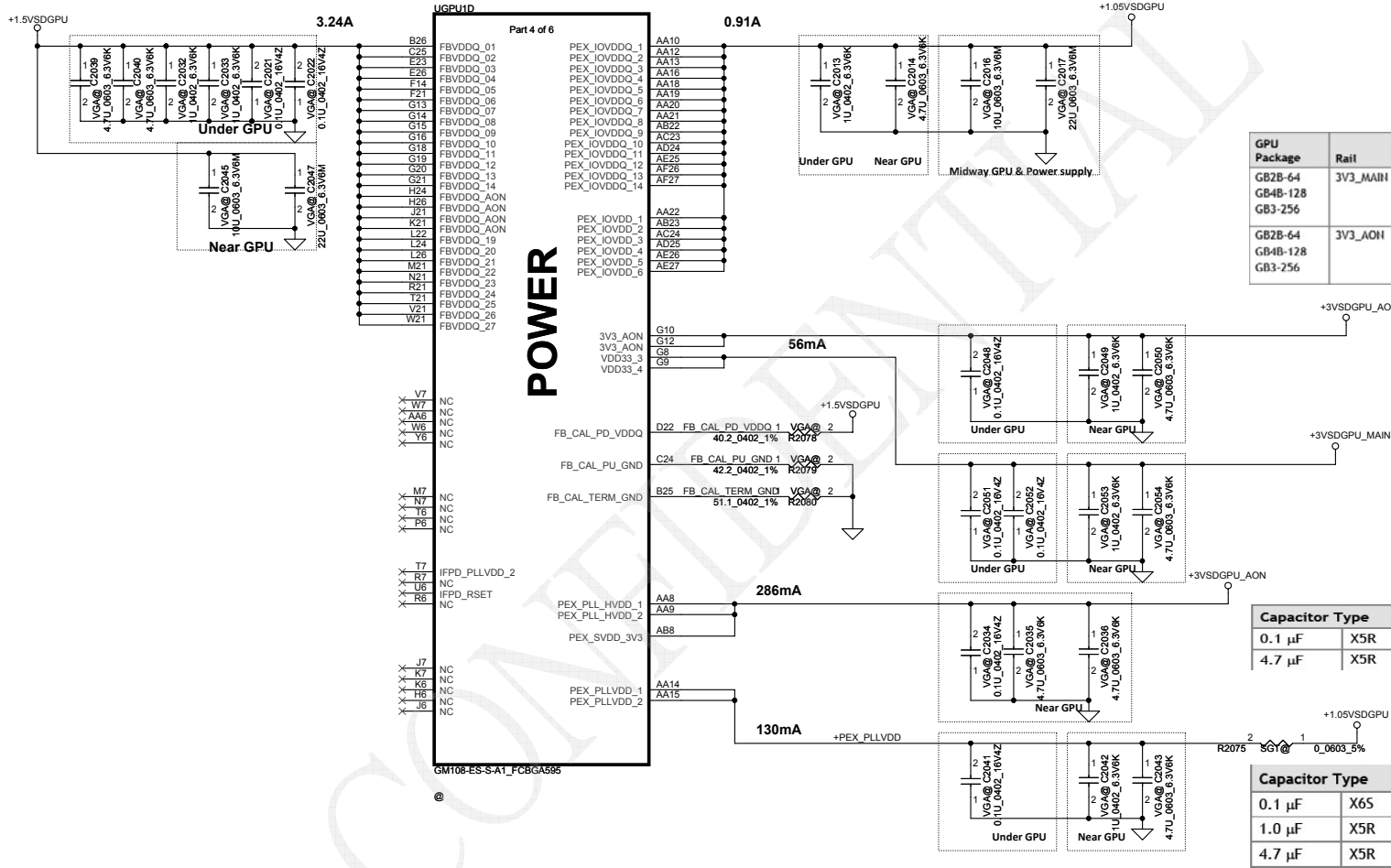
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2
		22 µF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)		0603	1
					Near GPU



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Hear GPU
	22µF	X5R 0805	1	Hear GPU

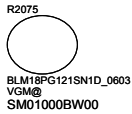
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0µF	X6S 0402	1	Under GPU
	4.7µF	X6S 0603	1	Hear GPU
	10µF	X5R 0805	1	Midway between GPU and Power Supply
	22µF	X5R 0805	1	Midway between GPU and Power Supply



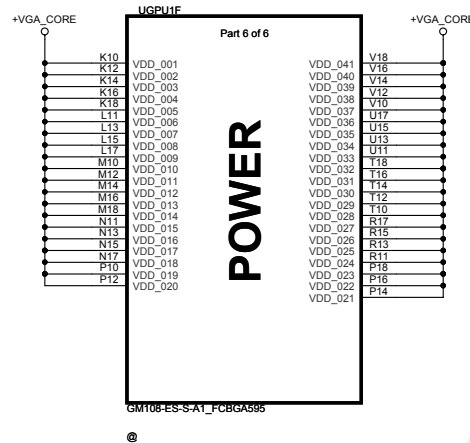
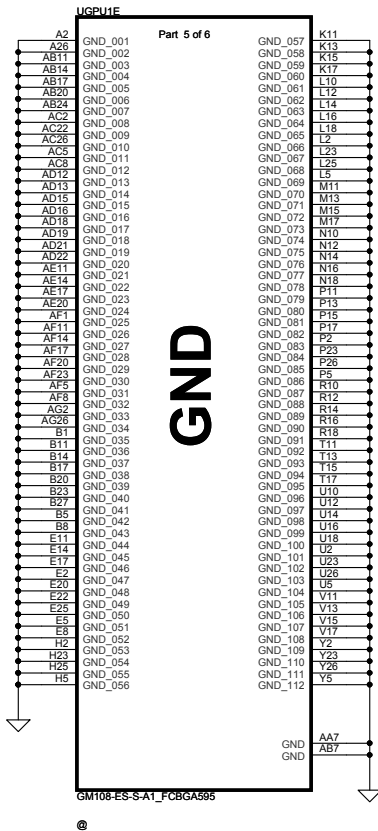
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S 0402	2	Under GPU
GB4B-128		1µF	X5R 0603	1	Hear GPU
GB3-256		4.7µF	X5R 0603	1	Hear GPU
GB2B-64	3V3_AON	0.1µF	X6S 0402	1	Under GPU
GB4B-128		1µF	X5R 0603	1	Hear GPU
GB3-256		4.7µF	X5R 0603	1	Hear GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X5R 0402	1	Near GPU
4.7µF	X5R 0603	2	Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X6S 0402	1	Under GPU
1.0µF	X5R 0603	1	Near GPU
4.7µF	X5R 0805	1	Near GPU



SM01000BW00 3000ma 120ohm@100mhz DCR 0.04



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU
	1 μ F	X6S	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at $T_j = 102^\circ\text{C}$

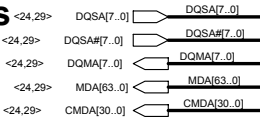
Power Supply Rail (V)	N15V-GM-S
	DDR3/L
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

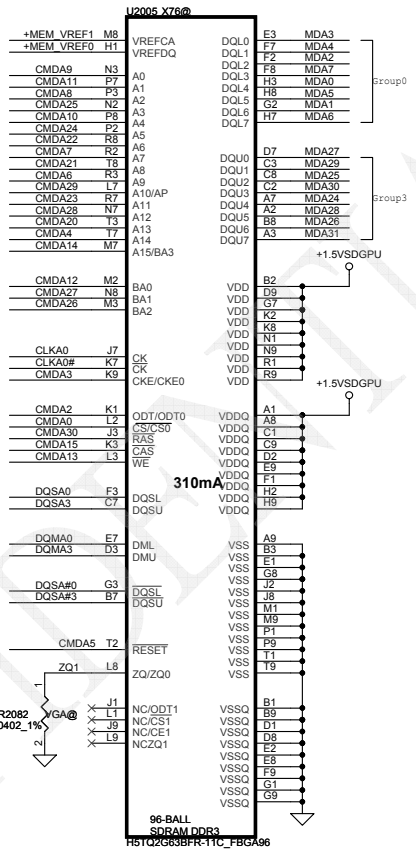
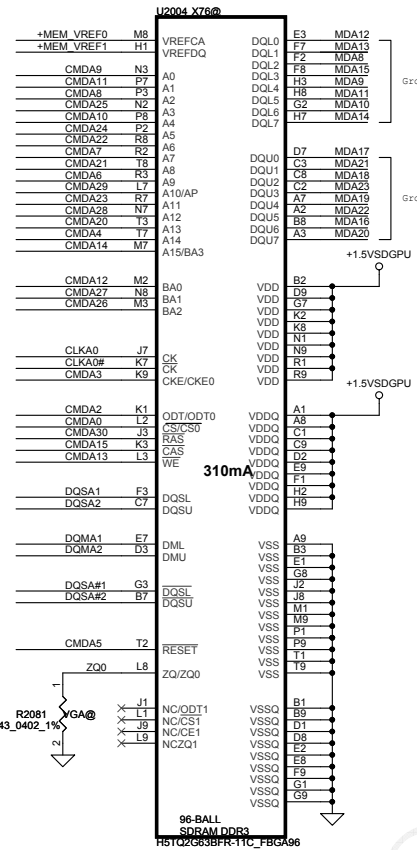
Table 7. EDP-Peak at $T_j = 102^\circ\text{C}$

Power Supply Rail (V)	N15V-GL
	DDR3
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips

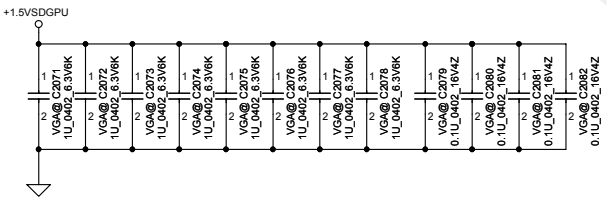


Upper 32

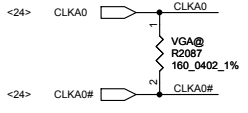
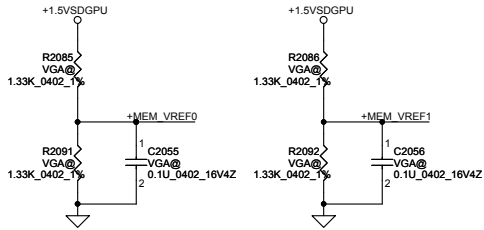


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

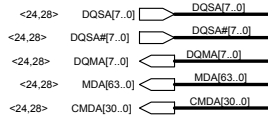
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



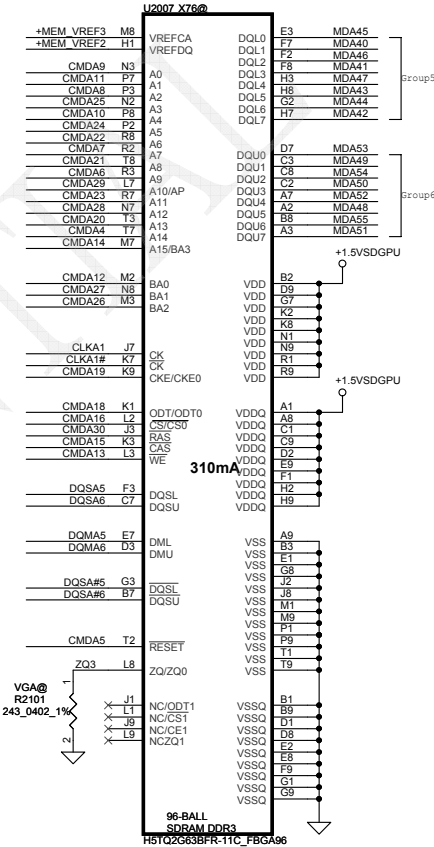
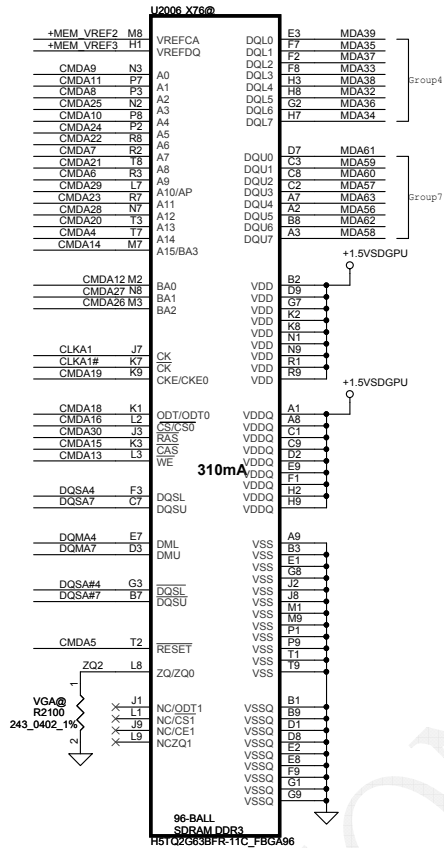
CMDA2	R2093	1	VGA@	2	10K	0402	5%
CMDA3	R2094	1	VGA@	2	10K	0402	5%
CMDA5	R2095	1	VGA@	2	10K	0402	5%
CMDA18	R2096	1	VGA@	2	10K	0402	5%
CMDA19	R2099	1	VGA@	2	10K	0402	5%



VRAM DDR3 chips

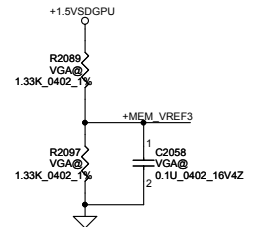
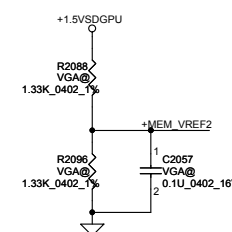
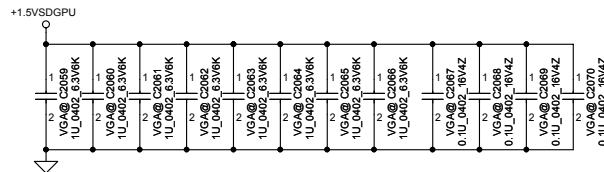
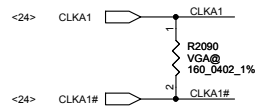


Lower 32

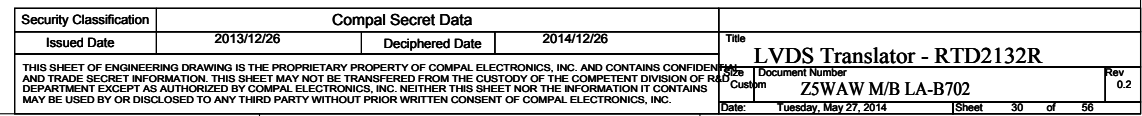


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

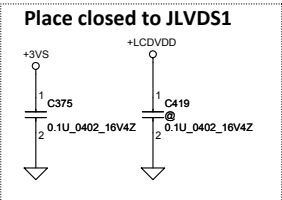
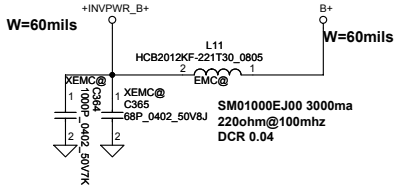
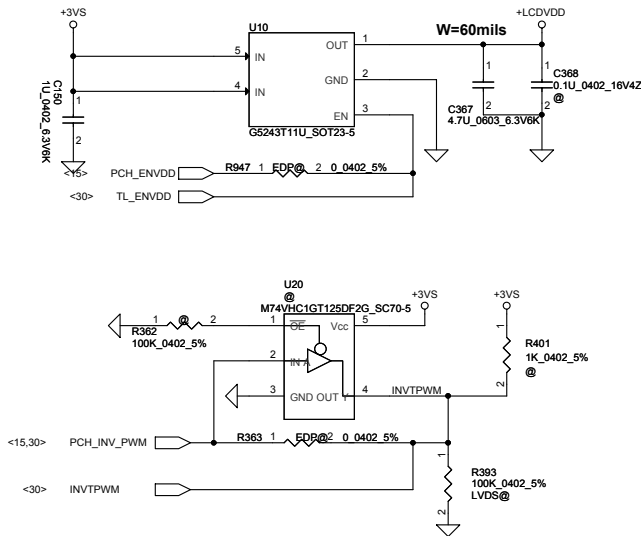


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Customer: ZSWAW M/B LA-B702				
Date: Tuesday, May 27, 2014				
Sheet 29 of 56				

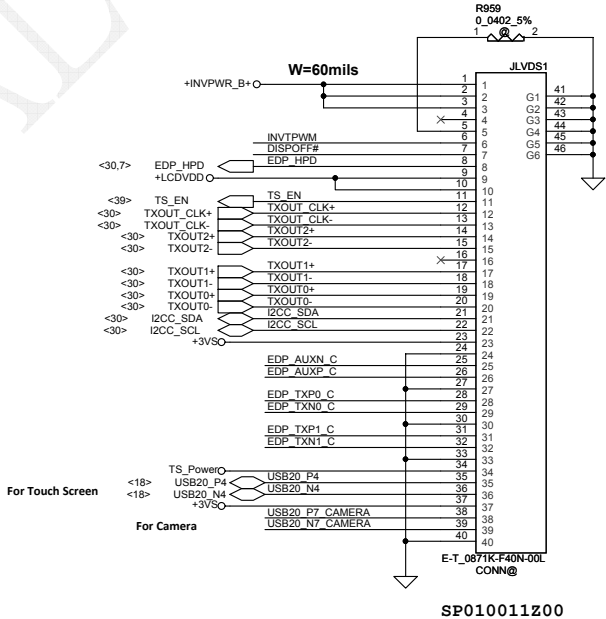
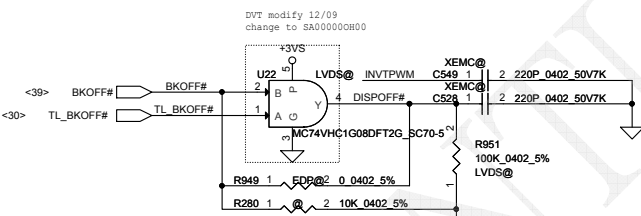
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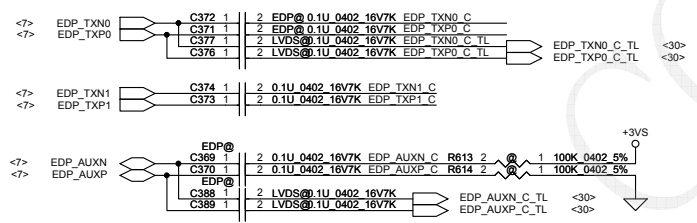
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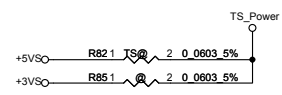
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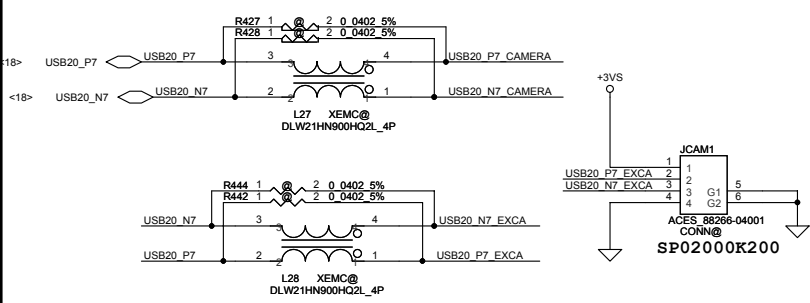
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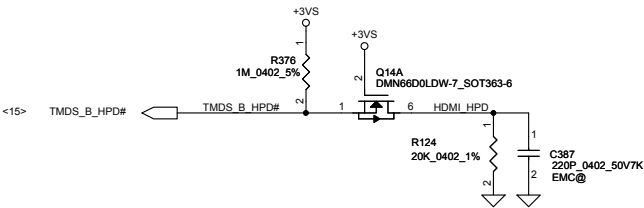
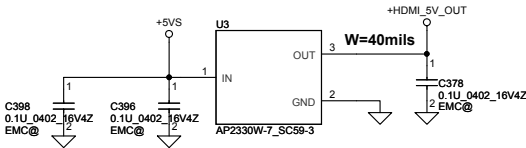
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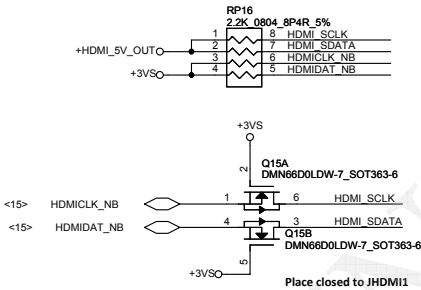
Camera



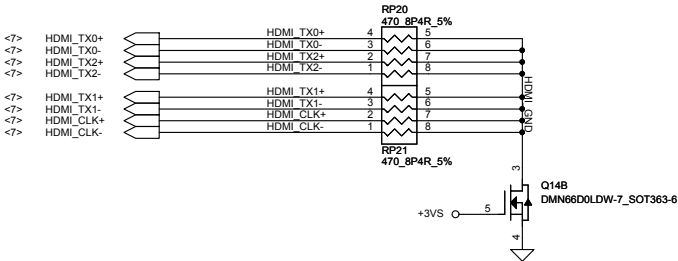
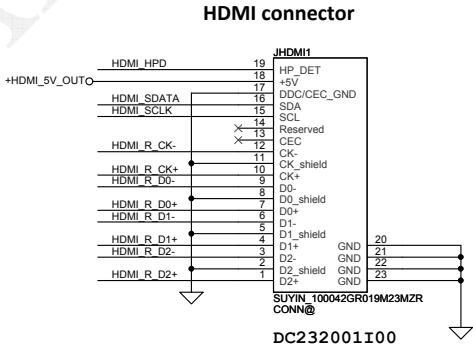
HDMI conn.



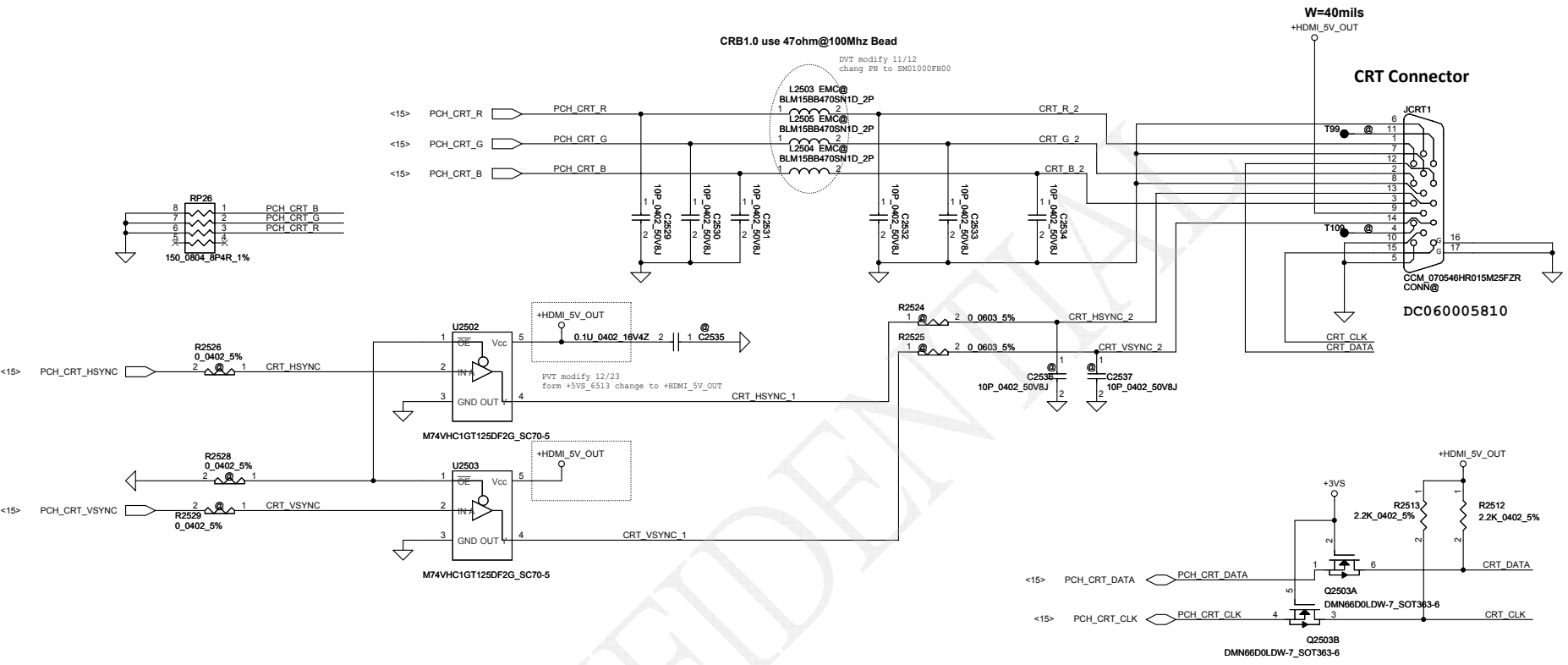
ZZZ1
HDMI ROYALTY
ROYALTY HDMI W/LOGO+HDCP
R00000003HM
45@



HDMI_CLK-	R368	1	XEMC@ 2 0 0402_5%	HDMI_R_CLK-
HDMI_CLK+	R369	1	XEMC@ 2 0 0402_5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@ 2 0 0402_5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@ 2 0 0402_5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@ 2 0 0402_5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@ 2 0 0402_5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@ 2 0 0402_5%	HDMI_R_D2-
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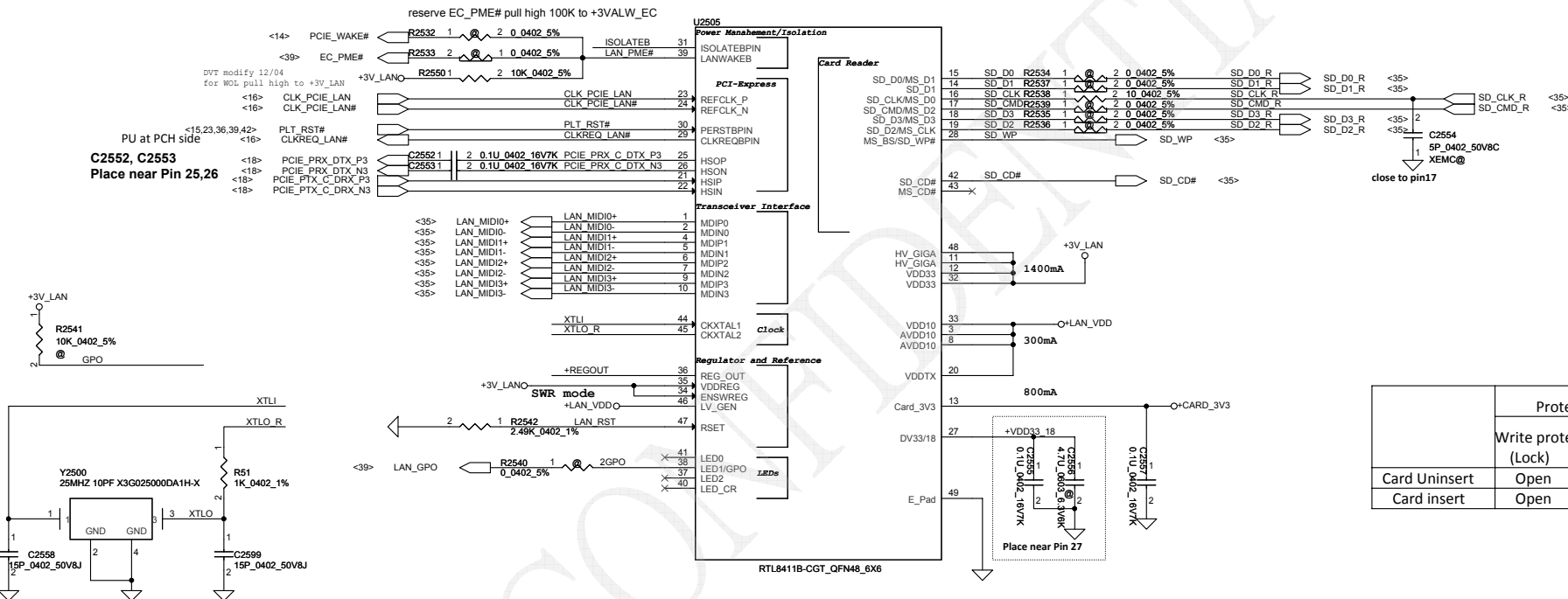
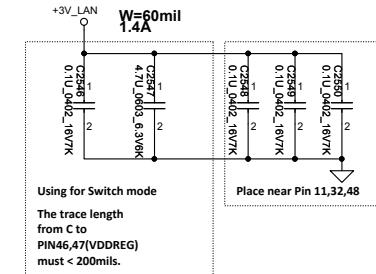
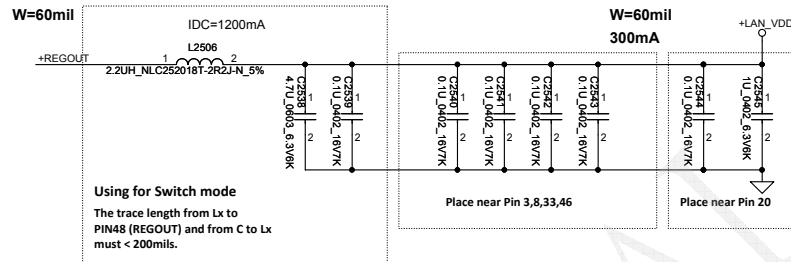
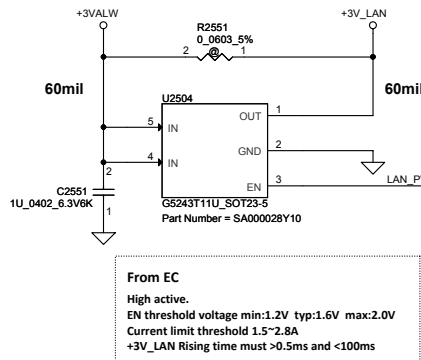


CRT conn.



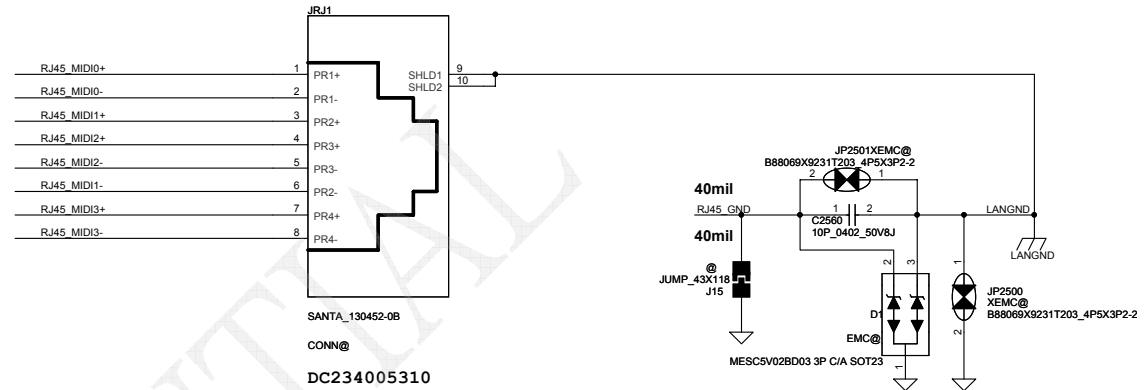
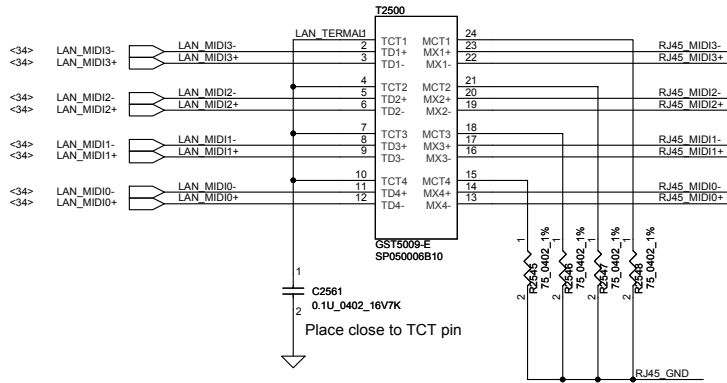
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				Doc No	Document Number	Rev
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				Date:	Tuesday, May 27, 2014	Sheet 33 of 56

LAN-RTL8411B

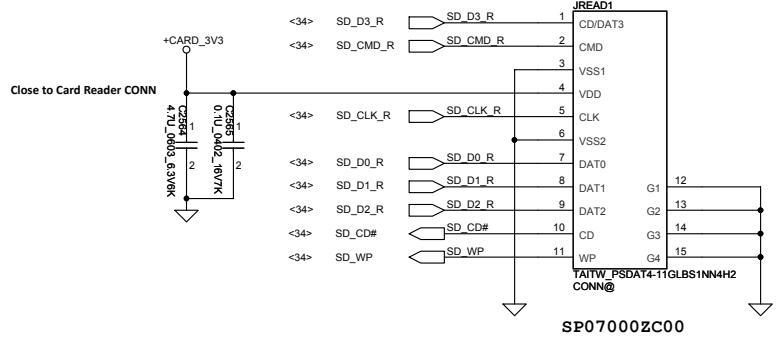


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

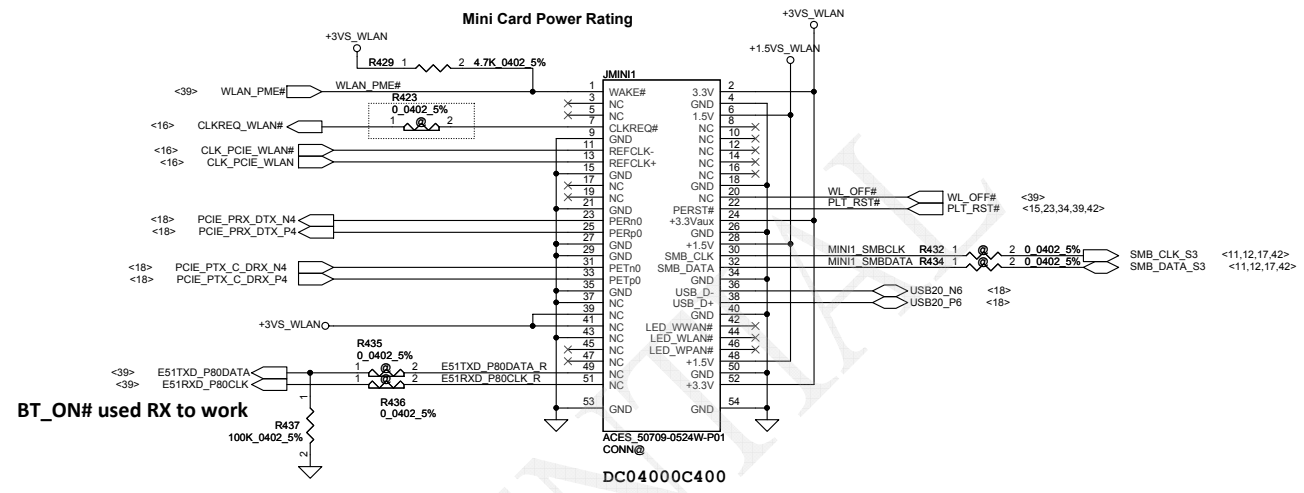
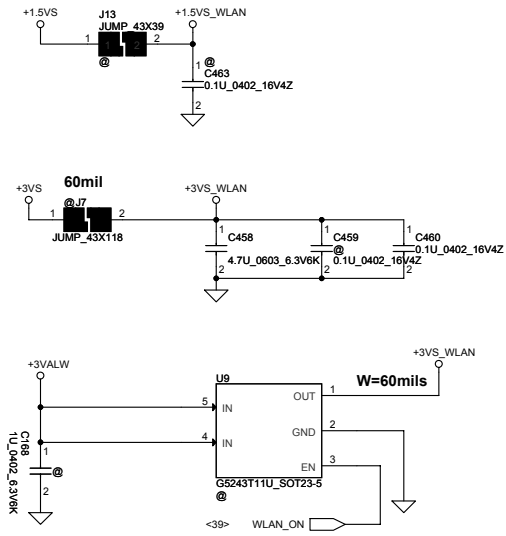
RJ45 / Card Reader conn.



Card Reader Connector

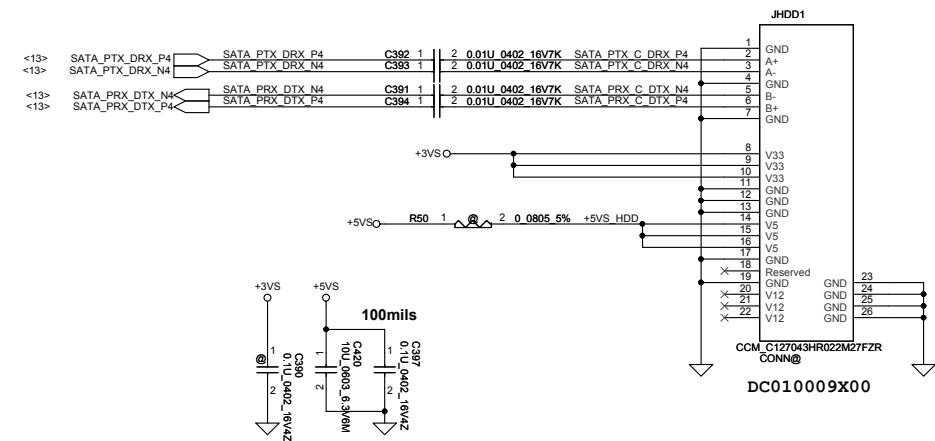


Wireless LAN

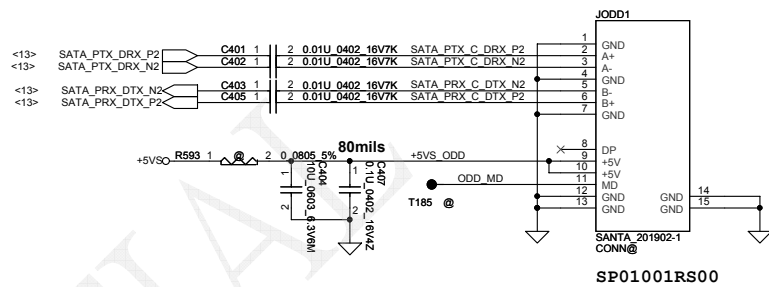


CONFIDENTIAL

SATA HDD1 Conn.

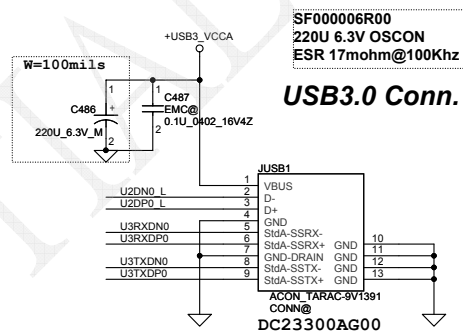
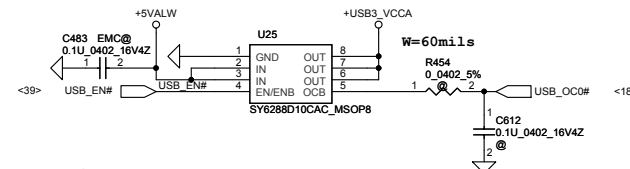
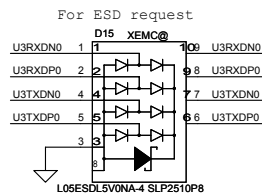
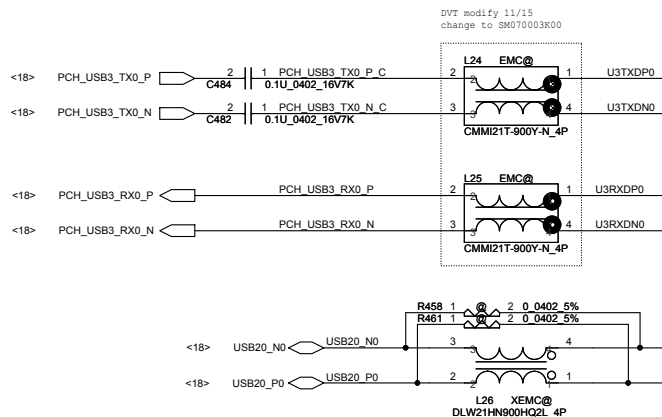


SATA ODD Conn.

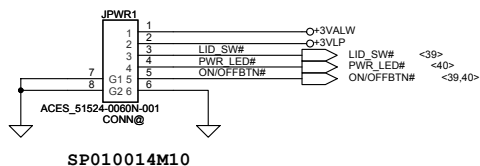


CONFIDENTIAL

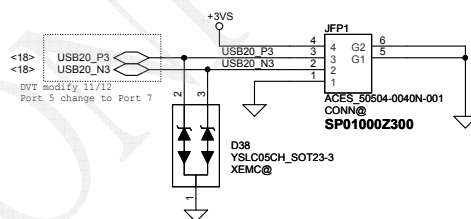
USB3.0 (Port 0)



PWR/B

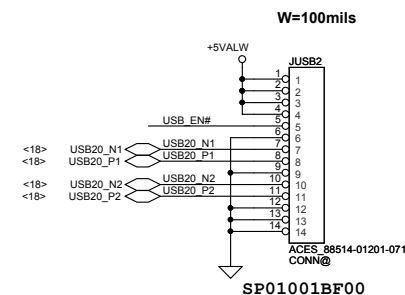


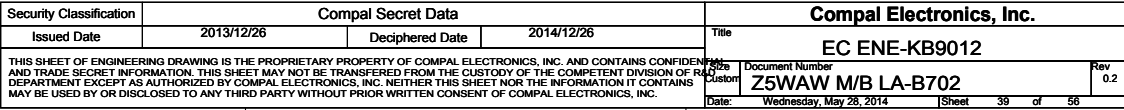
Finger Print /B for BA50



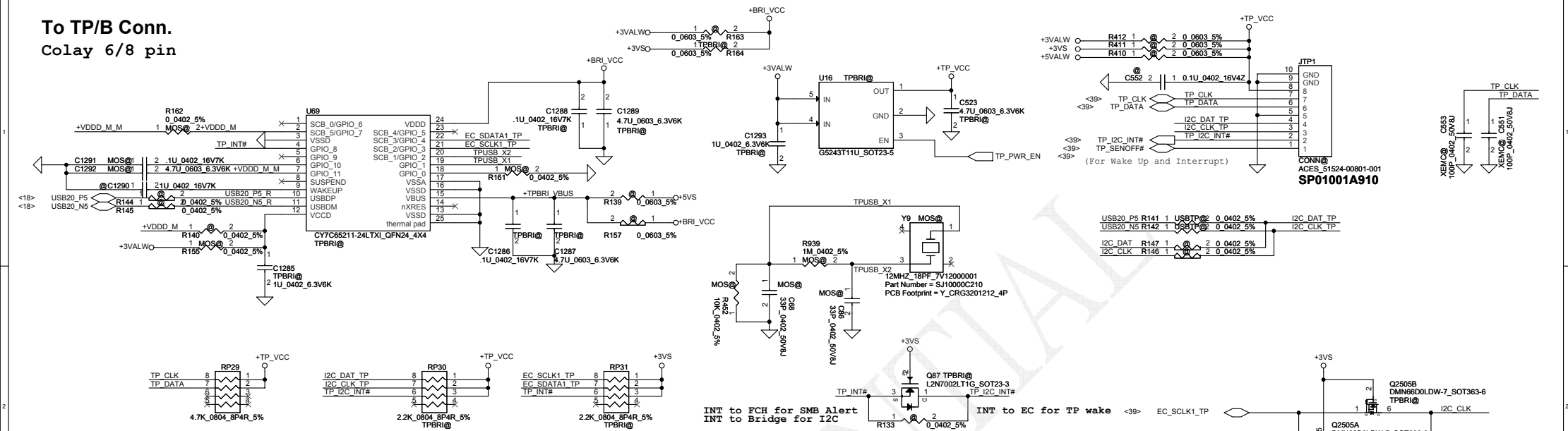
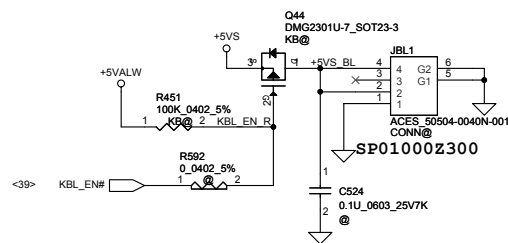
USB/B (USB Port 1, Port2)

USB/B Conn.





To TP/B Conn.
Colay 6/8 pin

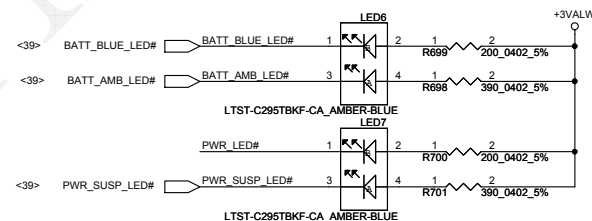
**KB BackLight Conn. Reserve**

NOTE :

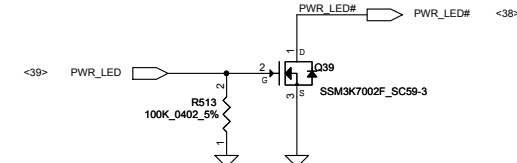
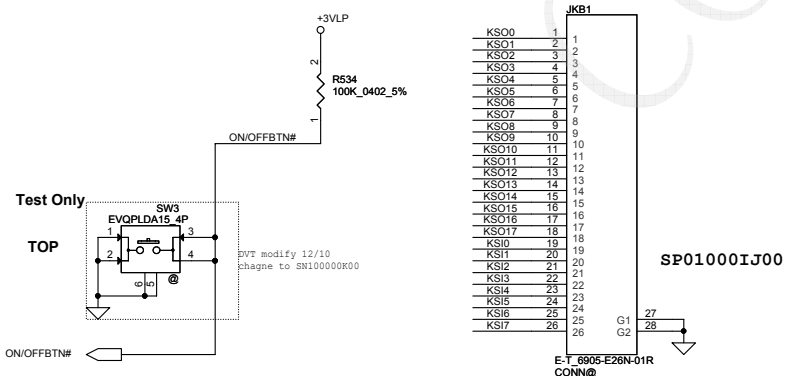
```
Cypress pop : TPBRI@
MOSART pop : TPBRI@ , MOS@ (default flash type)
EC I2C pop : R128,R129,R132,RP19
USBTP pop : USBTP@, (Q87 or R132, R130 option)
```



LED

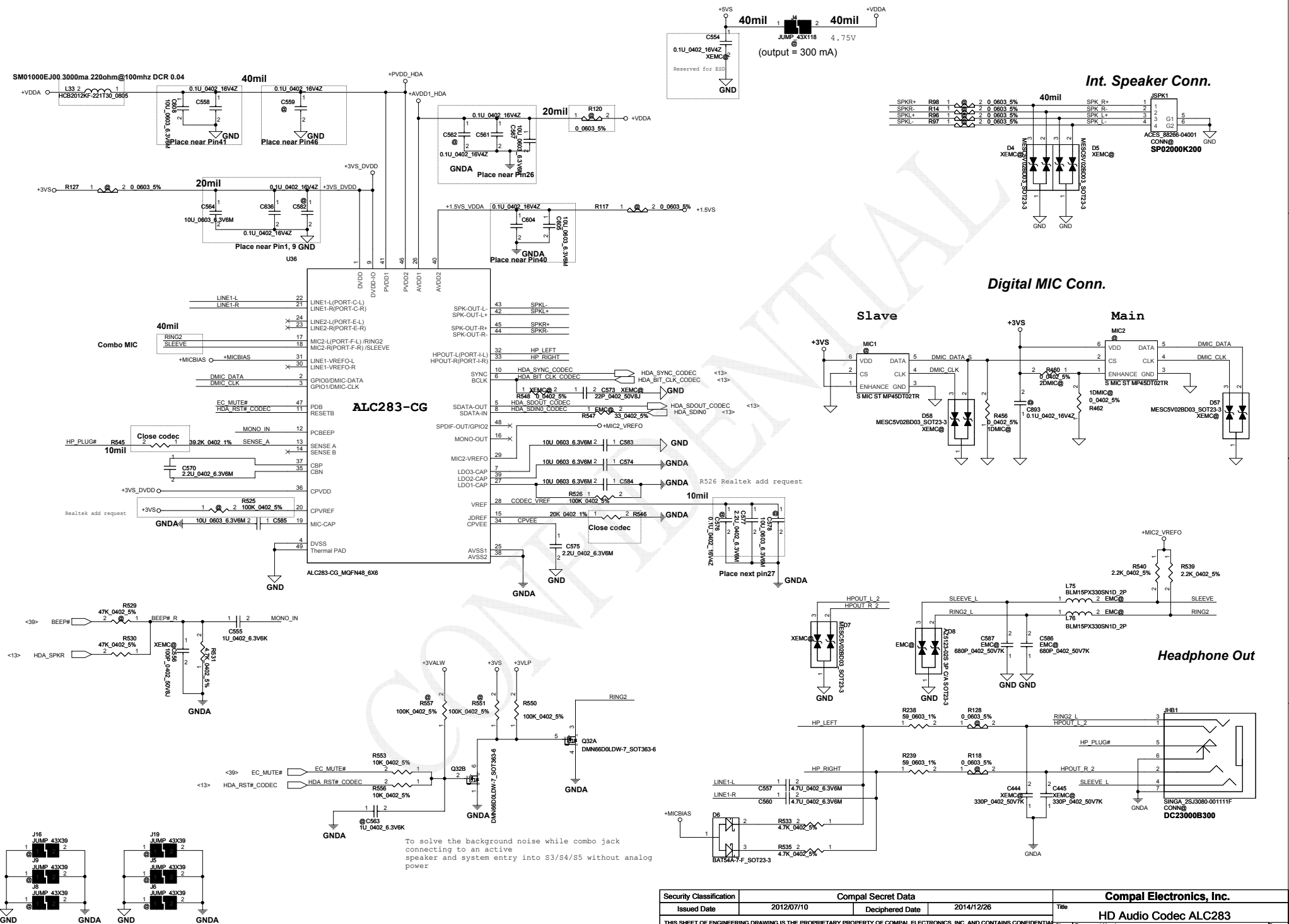


ON/OFF BTN

KB Conn.

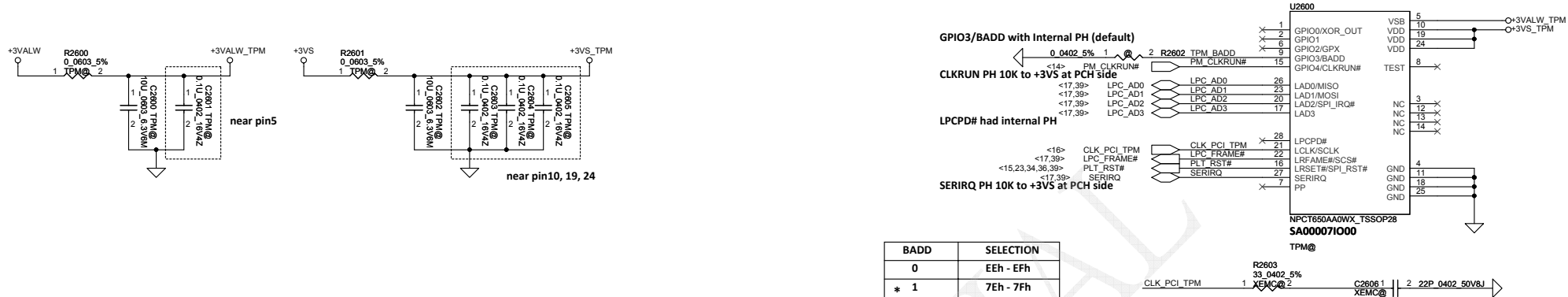
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	KB & TP & TPM Connector & LED	
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				Customer	Z5WAW M/B LA-B702	0.2
Date:	Tuesday, May 27, 2014	Sheet	40	of	56	

HD Audio Codec

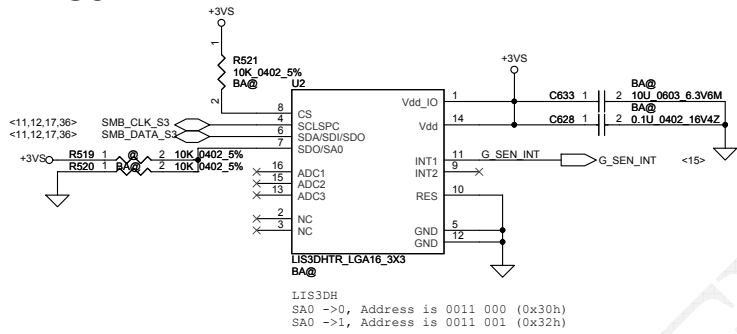


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					Z5WAW M/B LA-B702
				Rev	0.2
Date:				Tuesday, May 27, 2014	Sheet 41 of 56

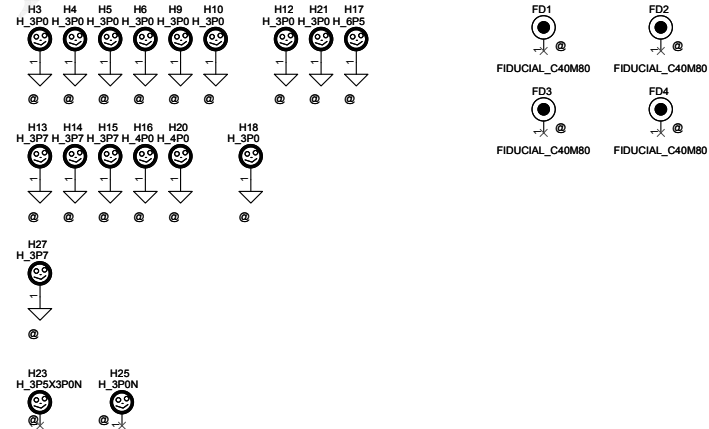
TPM Board for 2015



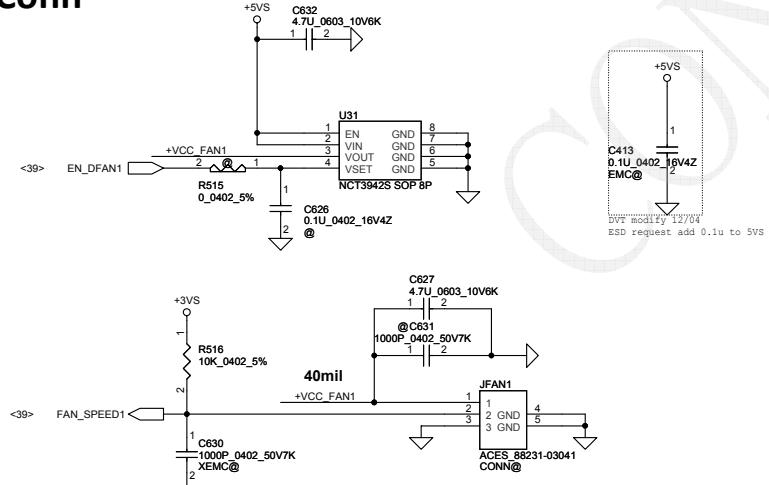
G-Sensor for BA50



Screw Hole

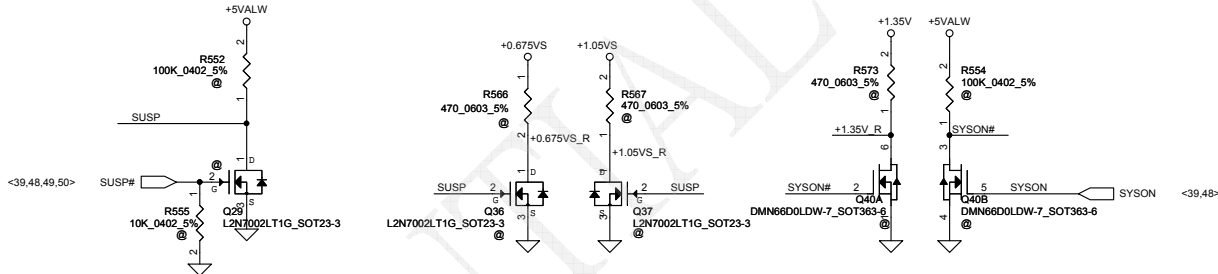
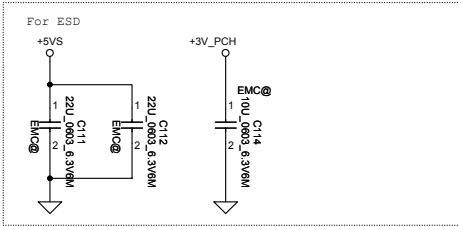
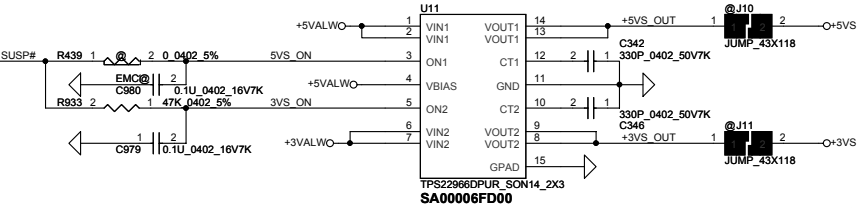
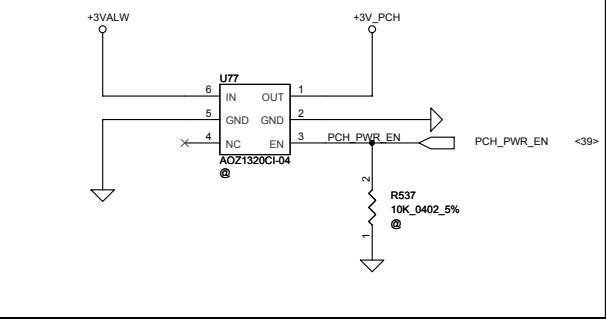


FAN1 Conn

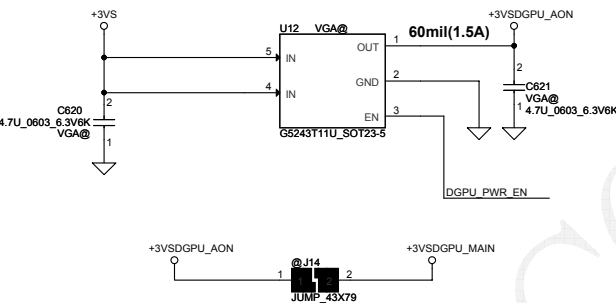


DC & VGA Interface

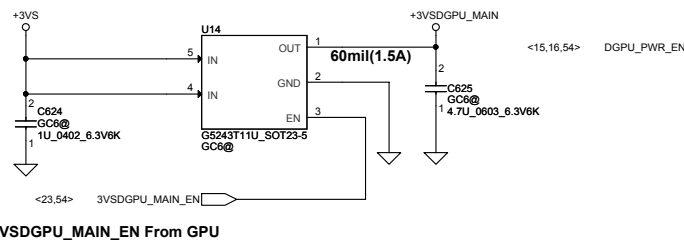
+3VALW to +3V_PCH Transfer



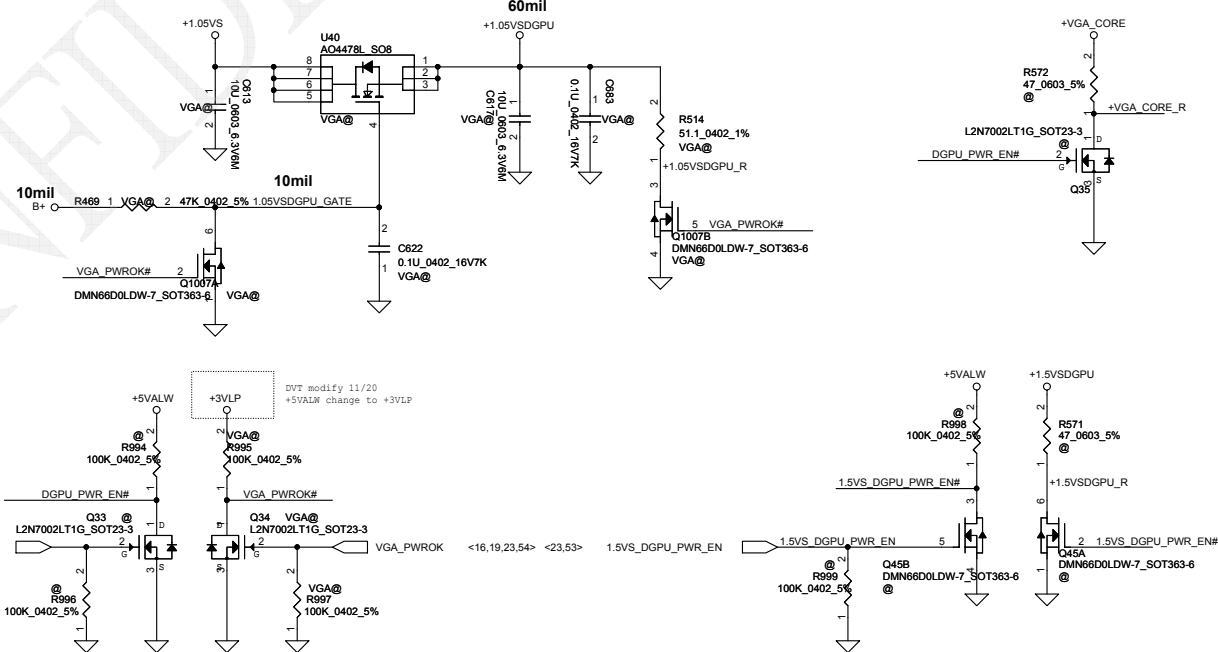
+3VS to +3VSDGPU_AON for GPU



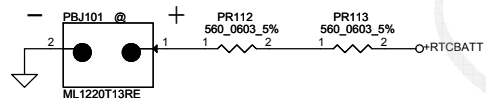
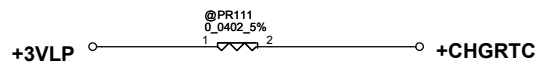
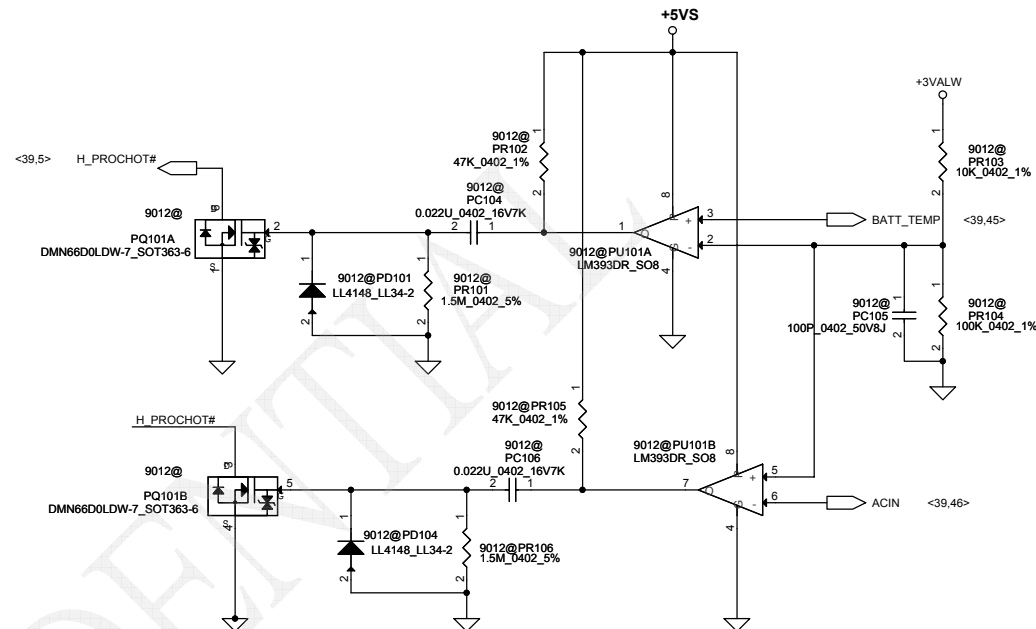
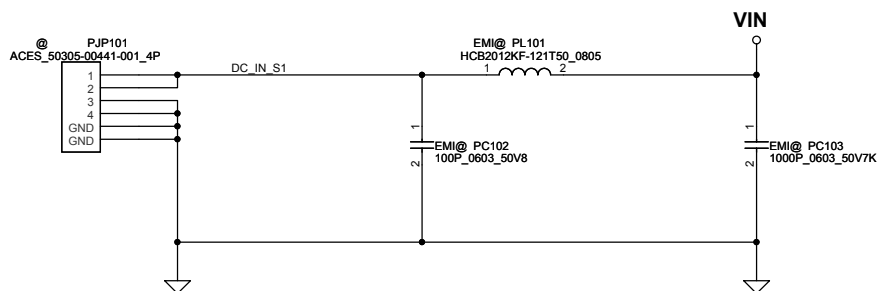
+3VS to +3VSDGPU_MAIN for GC6-2.0



+1.05VS to +1.05VSDGPU



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					Customer	
					Document Number	
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					Z55WAW M/B LA-B702	
					0.2	
Date:					Tuesday, May 27, 2014	
Sheet					43 of 56	



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				Document Number
				Rev 0.1
				Date: Tuesday, May 27, 2014
				Sheet 44 of 56

BQ24735A V2.mdd

	Vin Detector		
	Min.	Typ	Max.
L-->H	17.52V	18.01V	18.50V
H-->L	16.97V	17.59V	18.24V

$$\begin{aligned} \text{VILIM} &= 20 \cdot \text{ILIM} \cdot \text{Rsr} \\ \text{ILIM} &= 3.3 \cdot 100 / (100 + 316) / 20 / 0.02 \\ &= 4.006 \text{ A} \end{aligned}$$

```

003 16V/K
**Design Notes**
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. Disable turbo when AC only
#Circuit Design
1. ACOR,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L side MOSFET
    Charge current 3.5A
    Power loss : 1.82W
    Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit
for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors
with PR222 for ACDET setting)
4. PC223 2200p is for quick response when AC plug out.
5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating
#Protect function
1. ACOVF : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCF : 3/4.5/6A based on current current setting
5. BATOVF : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 110mV (default)

```

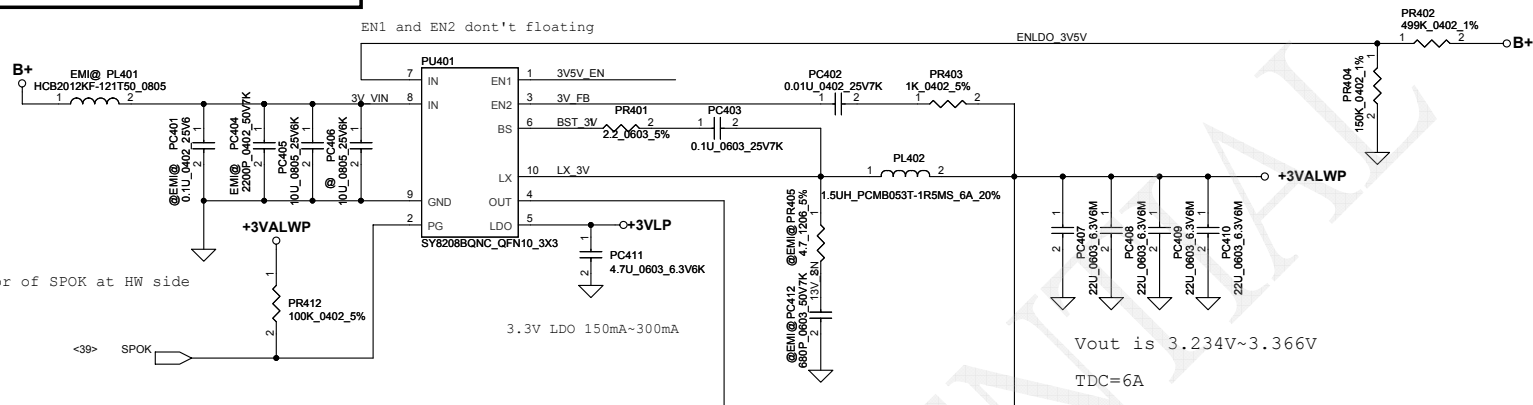
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/12/26	Deciphered Date	2014/12/26	CHARGER		
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				Docuement Number	Common Circuit	
				Date:	Tuesday, May 27, 2014	Sheet 46 of 56
						Rev 0.1

Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

EN1 and EN2 don't floating

ENLDO_3V5V



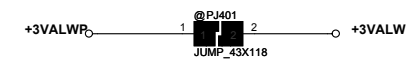
Check pull up resistor of SPOK at HW side

<39> SPOK

3.3V LDO 150mA~300mA

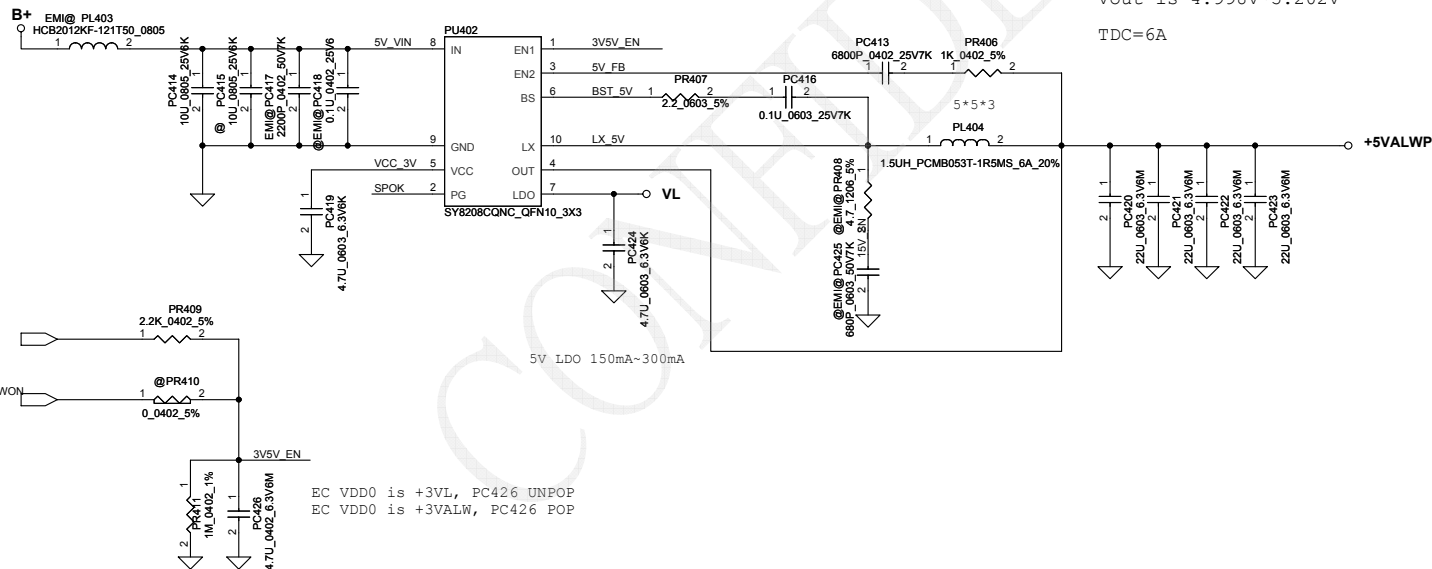
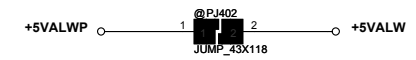
Vout is 3.234V~3.366V

TDC=6A



Vout is 4.998V~5.202V

TDC=6A



5V LDO 150mA~300mA

EC VDD0 is +3VL, PC426 UNPOP
EC VDD0 is +3VALW, PC426 POP

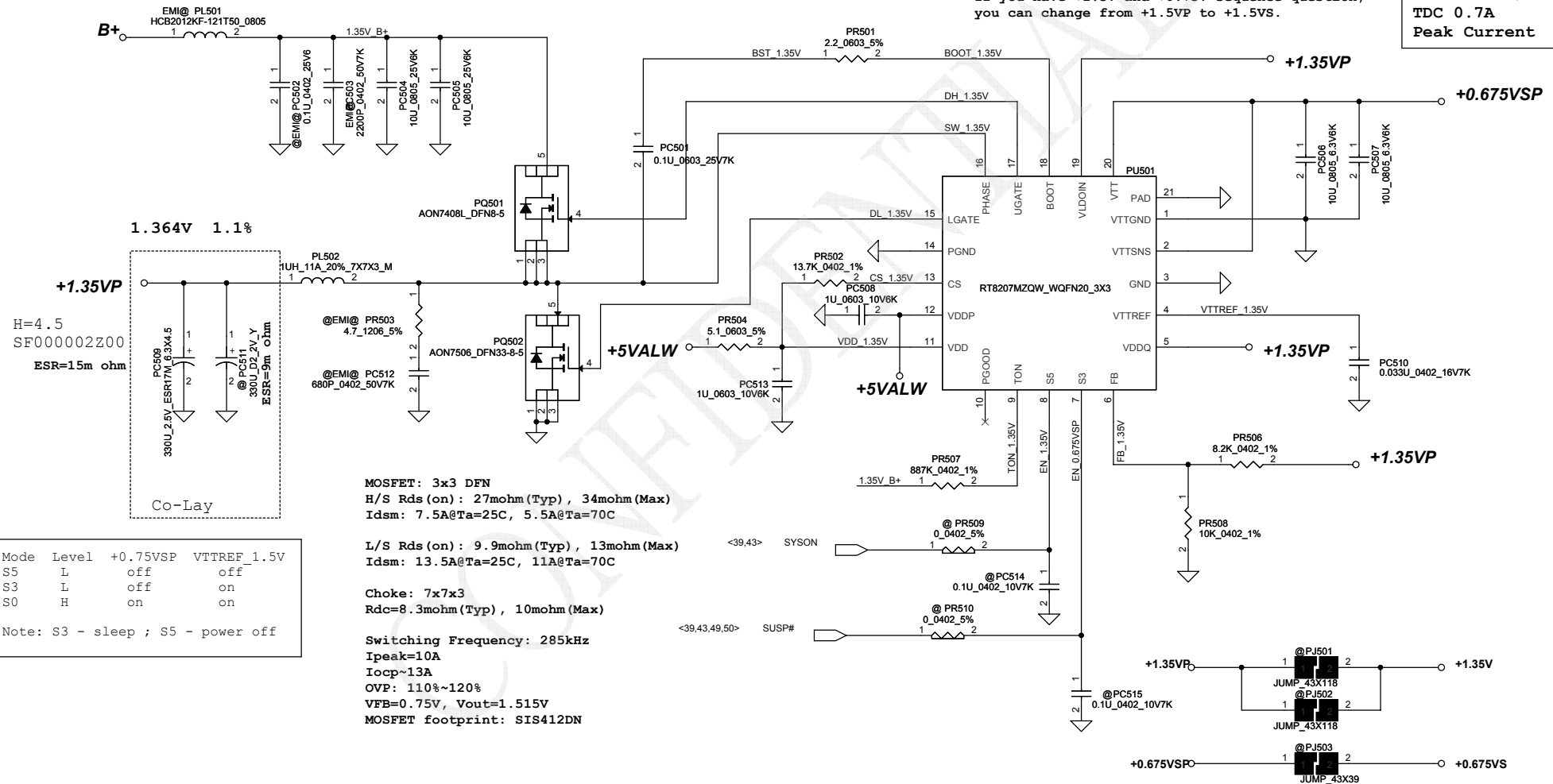
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Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	+3VALW/+5VALW
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				Date	Tuesday, May 27, 2014
				Sheet	47 of 56

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

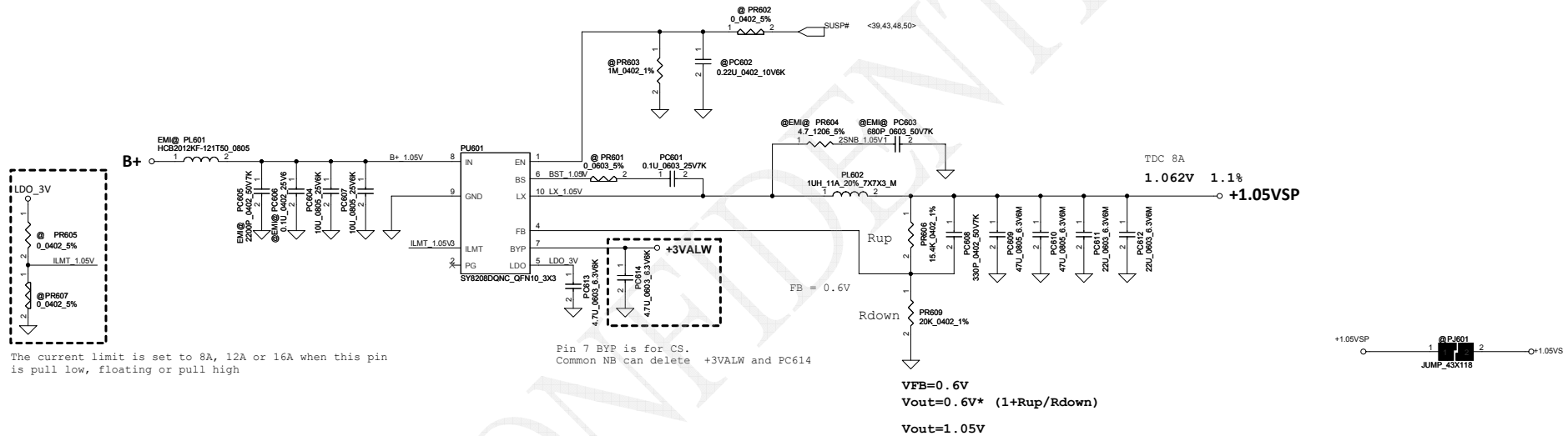
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

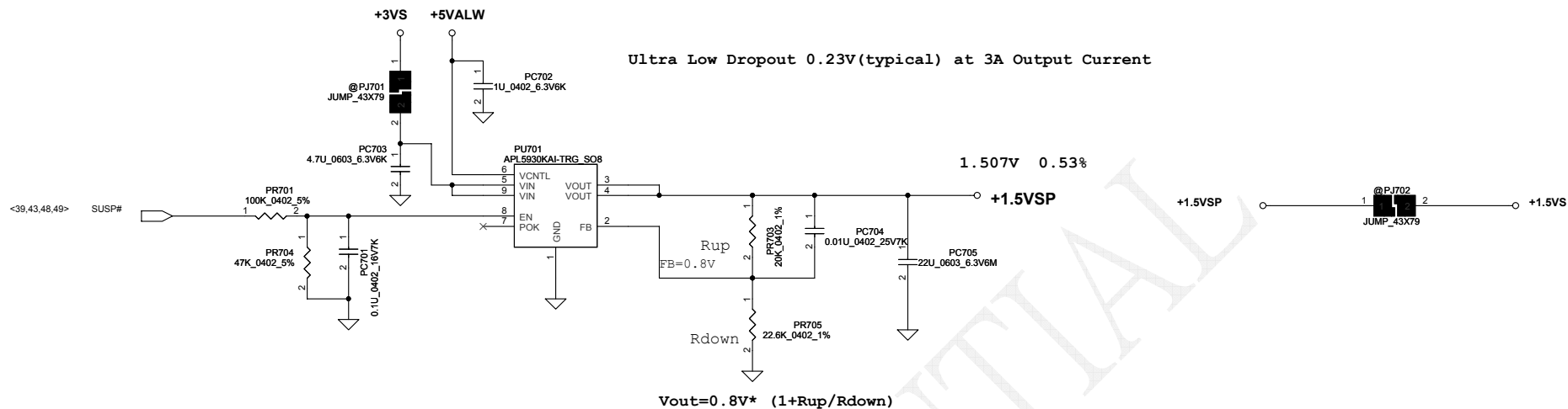


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				Date:	Tuesday, May 27, 2014
				Sheet	48 of 56

Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR603

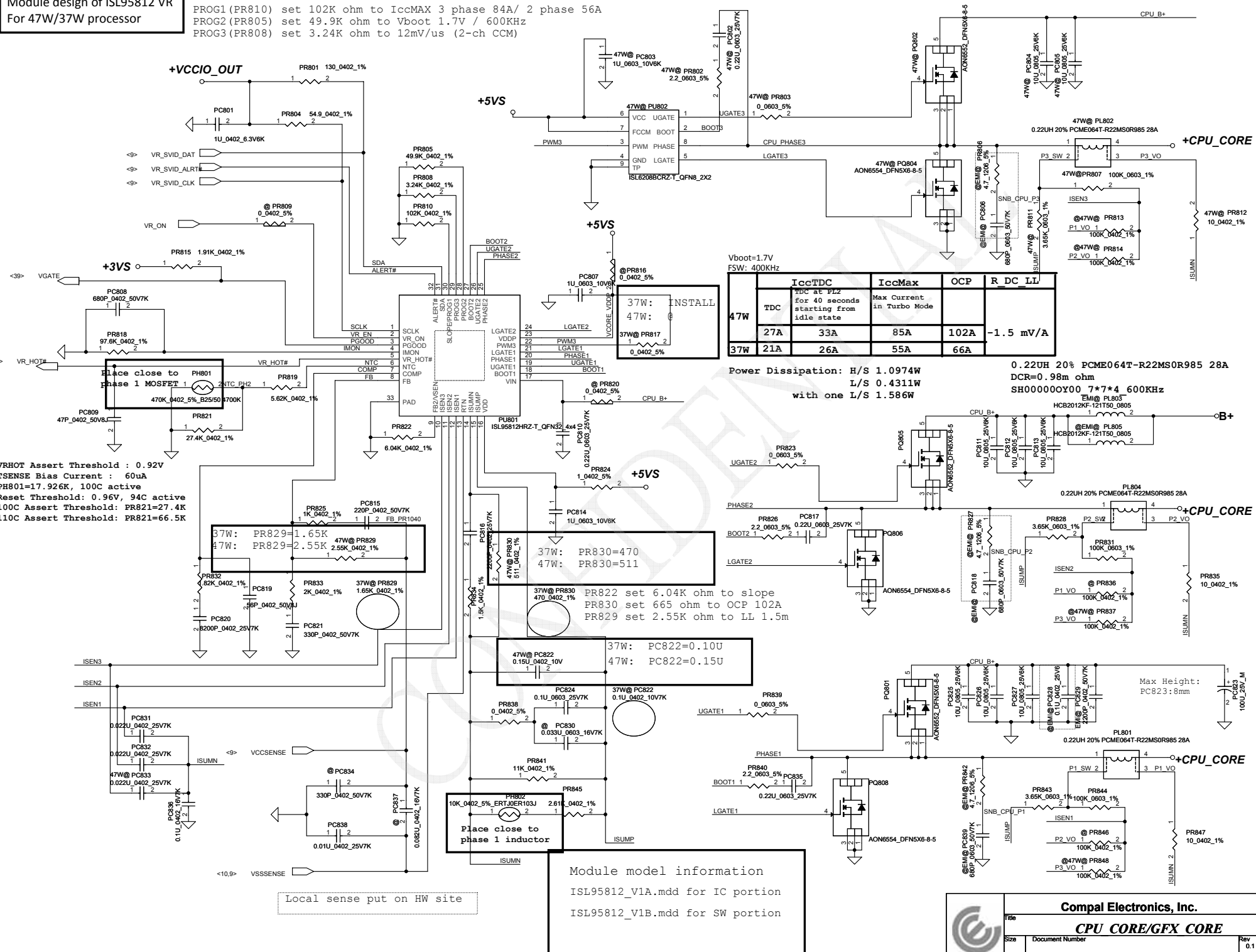




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				Document Number
				Rev
				0.1
				Date
				Tuesday, May 27, 2014
				Sheet
				50
				of
				56

**Module design of ISL95812 VR
For 47W/37W processor**

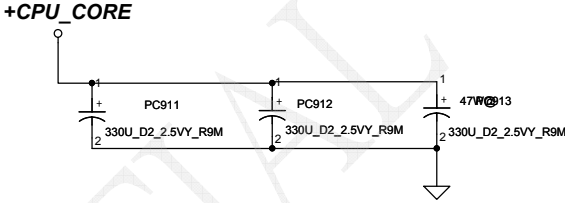
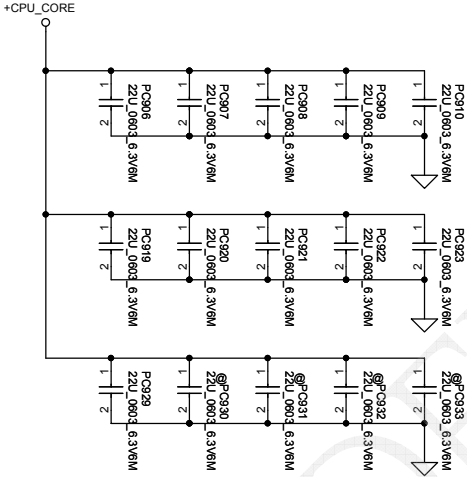
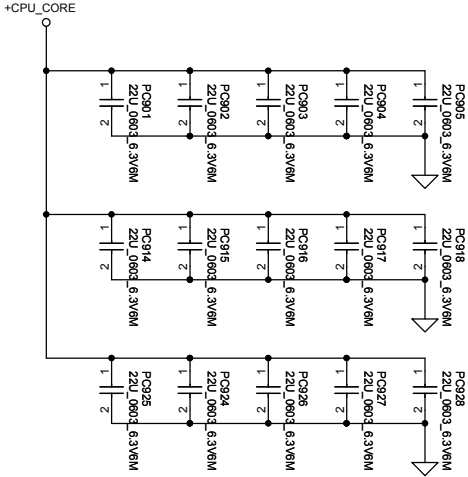
PROG1(PR810) set 102K ohm to IccMAX 3 phase 84A/ 2 phase 56A
PROG2(PR805) set 49.9K ohm to Vboot 1.7V / 600KHz
PROG3(PR808) set 3.24K ohm to 12mV/us (2-ch CCM)



PWR Rule
需確認最新SPEC.
Modify 8/6.

3 X 330u/9m (47W)
2 X 330u/9m (37W)
24 pcs 22uF and reserve 4 pcs
2013/08/16

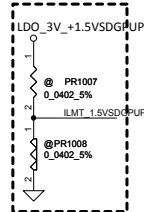
2 X 330u/9m (47W)
26 pcs 22uF
2013/08/28



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				Custom	Rev
				Date	0.1
				Tuesday, May 27, 2014	1 Sheet 52 of 56

```
Module model information
SY8208D_v1.mdd
```

EN pin don't floating
If have pull down resistor at HW side, pls delete PR1002



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC614

$$V_{FB} = 0.6V$$
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$
$$V_{out} = 1.05V$$

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				Date:	Tuesday, May 27, 2014	Sheet 53 of 56

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

$V_{boot} = V_{vref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C	Config D
Vmin	0.6V	0.6V	0.65V	0.9V
Vmax	1.2V	1.2V	1.15V	1.15V
Vboot	0.875V	0.9V	0.9V	1.028V
Voltage step	6.25mV	6.25mV	25mV	12.5mV
N of Voltage level	96	96	20	20
PWM Frequency	1.125	1.125	0.676	0.676
Rrefadj	PR1206	39K	20K	39K
Rref1	PR1204	39K	20K	30K
Rboot	PR1205	1.5K	2K	3K
Rref2=PR1209+PR1212	PR1209	30K	18K	24K
	PR1212	1.5K	0	3K
C	PC1209	1.5nf	2.7nf	1.8nf

Current Limit threshold setting
 $R_{oset} = (V_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10uA$

$I_{ripple} = (19 - 0.9) * 0.9 / (304.89KHz * 0.36uF * 19) = 7.811A$

OCP=54A/2=27A per phase
 $I_{valley} = 27A - 7.811A/2 = 23.1A$

H-side MOS: AON6552
 $R_{ds(on)} = 5.6m\Omega @ V_{gs} = 10V$
 $6.7m\Omega @ V_{gs} = 4.5V$
 $I_{d_20A} @ T_a = 25 \text{ degC}$

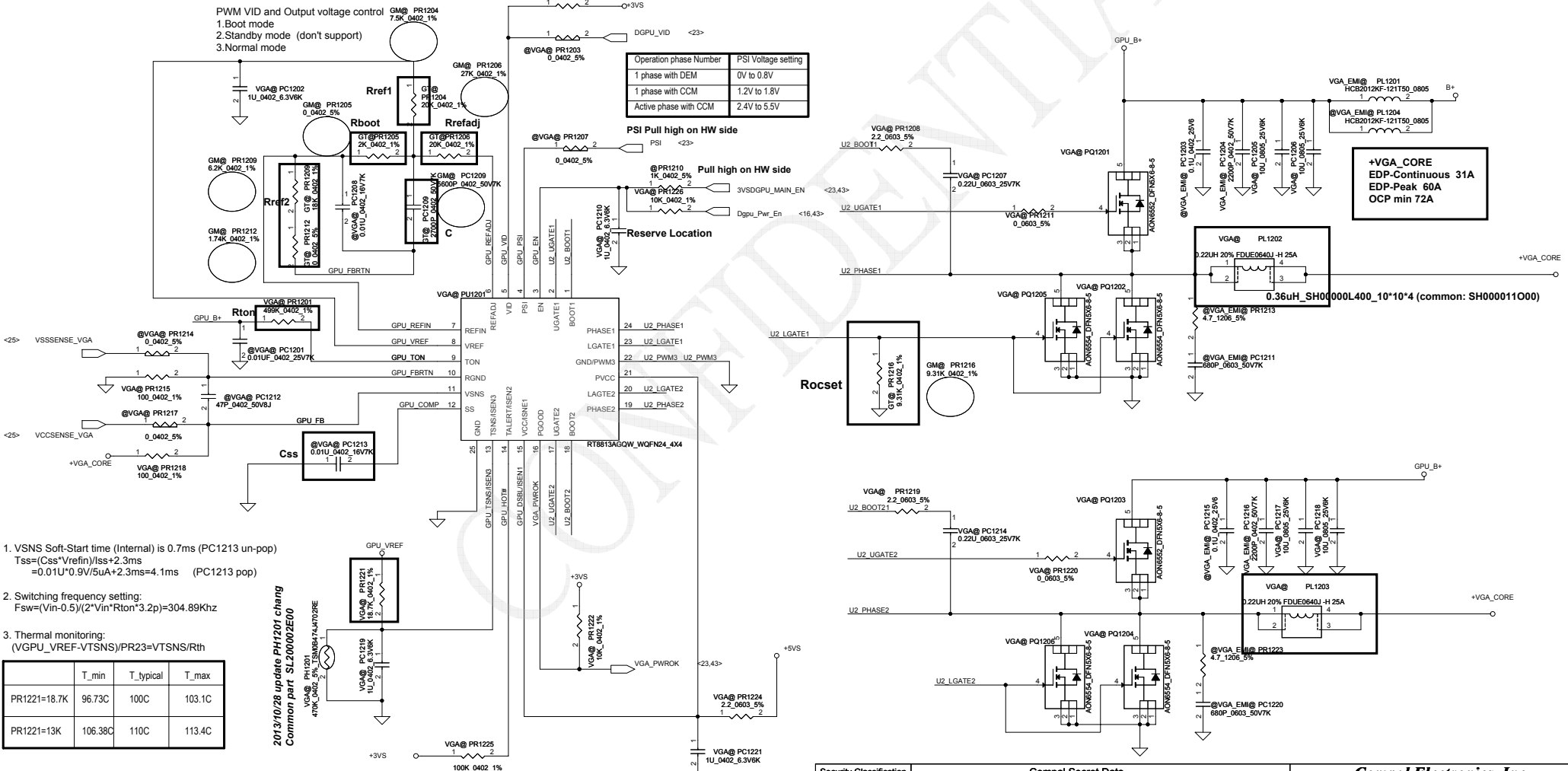
L-side MOS: AON6554
 $R_{ds(on)} = 3.2m\Omega @ V_{gs} = 10V$
 $3-3.8m\Omega @ V_{gs} = 4.5V$
 $I_{d_85A} @ T_a = 25 \text{ degC}$

Choke: 0.36uH (Size: 10*10*4)
 $R_{dc} = 0.82m\Omega @ \pm 5\%$
Heat Rating Current=37A
Saturation Current=40A

$C = 3 * 330uF (9m\Omega) = 990uF$
 $V_{ripple} = I_{ripple} * ESR_{(min)} = 7.811A * 3m\Omega = 23.4mV$

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config D
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



1. VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3ms$
 $= 0.01uF * 0.9V / 5uA + 2.3ms = 4.1ms$ (PC1213 pop)

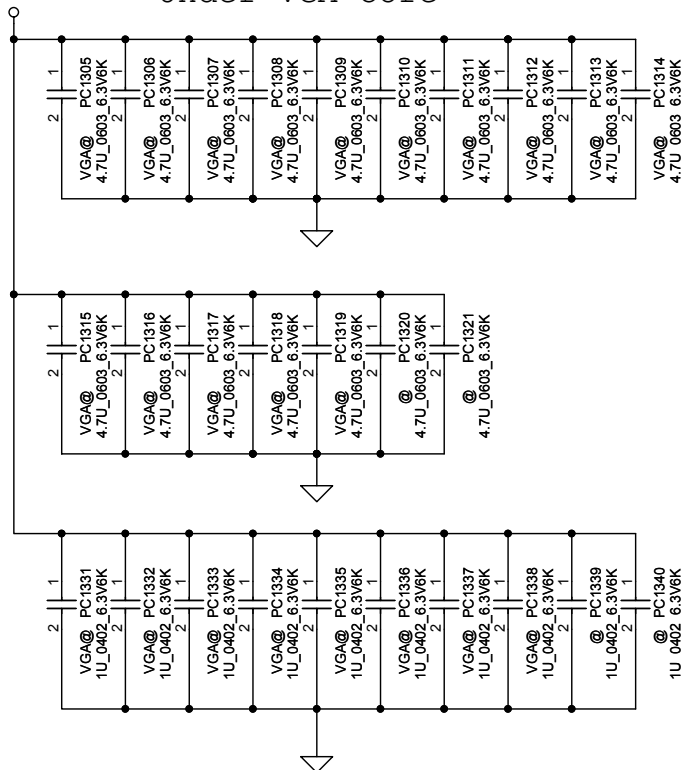
2. Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p) = 304.89KHz$

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR23=VTSNS/Rth

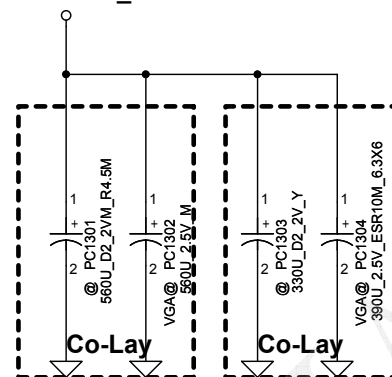
	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C

2013/10/28 update PH1201 chang
Common part SL20002E00

+VGA_CORE Under VGA Core



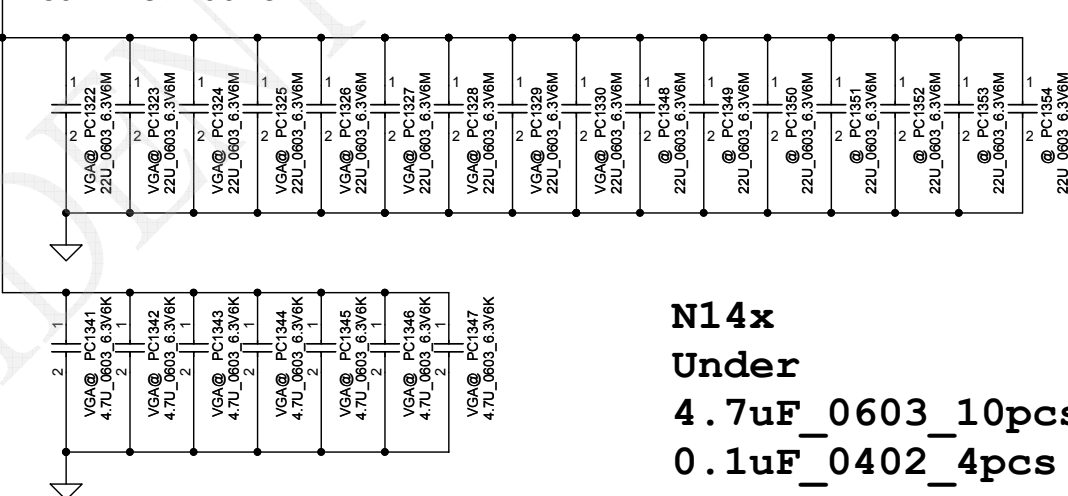
+VGA_CORE



N15x
Under
4.7uF_0603_15pcs stuff 2
1uF_0402_8pcs stuff 2
Near
47uF_0805_0pcs
22uF_0805_14pcs stuff 7
4.7uF_0805_5pcs stuff 2

+VGA_CORE

Near VGA Core



N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title	
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				Custom	0.1
Date: Tuesday, May 27, 2014				Sheet	55 of 56

VGA_CORE CAP

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1		Reduce 0 ohm count		Change PR510, PR602, PR607, PR809, PR816, PR820 to R-short	4/1	DVT
2	HW request	Change VRAM voltage to raise VRAM sequence	53	Change PR1006 to SD034240280	4/1	DVT
3		Improve CPU transient	51	Change PR818 to SD034976280	4/1	DVT
4		Reduce 0 ohm count		Change PR601, PR1001, PR1003, PR1008 to R-short	5/2	PVT
5		Component PN from M0 to 80	51	Change PC820 PN from SE0000006M0 to SE000000680	5/5	PVT
6		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6414 change to AON6508	5/5	PVT
7		CPU TAT show VR thermal Alrt	51	change PR819 from 3.42K to 5.62K (active from 96'C to 106'C)	5/12	PVT
8		slewrate from ULV change to SV	51	PR808 from 16.9K to 3.24K (from 53mV/us to 12mV/us)	5/12	PVT
9		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6508 change to AON6554	5/15	PVT MEMO
10		Thermal team change PH1 setting	45	PR216 from 16.9K to 26.1K (92'C active change to 85'C active)	5/15	PVT MEMO
12						
13						
14						
15						
16						
17						

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Date: Tuesday, May 27, 2014				Sheet 56 of 56	